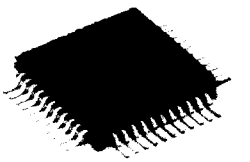
M51581FP/GP
DIGITAL AUDIO INTERFACE (DAI)

DESCRIPTION

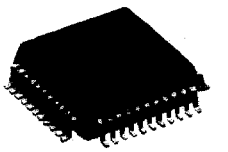
The M51581 is a semiconductor IC for transmitting and receiving signals formed according to a digital audio interface format conforming to the EIAJ standards. It has a variety of functions as it supports both professional and consumer modes and can be applied to the serial copy management systems (SCMS). The IC enables the engineer to configure an optimum digital audio interface for DAT, DCC, MD, and CD-R systems.

FEATURES

- Capable of dealing with audio data up to 24-bit
- Adaptable to both the I²S and non-I²S audio interface formats
- Selection available from three kinds of control methods (microcomputer, easy, and full-transparent modes)
- Two channels of signal input pins for reception
- Feedthrough function equipped
- Level converter for converting the level of received signals into CMOS level (minimum input level : 200mVp-p)
- Supports both consumer and professional modes



Outline 44P6W-B(FP)
1.0mm pitch QFP
(13.2mm × 13.2mm × 2.0mm)

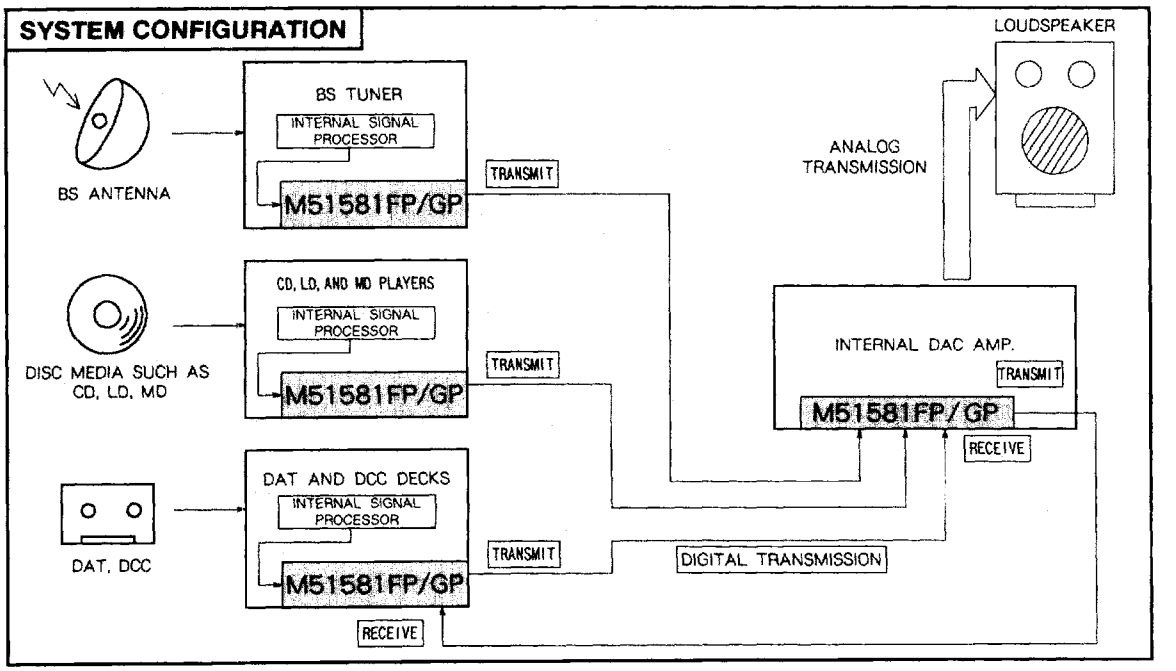


Outline 44P6N-A(GP)
0.8mm pitch QFP
(10.0mm × 10.0mm × 2.8mm)

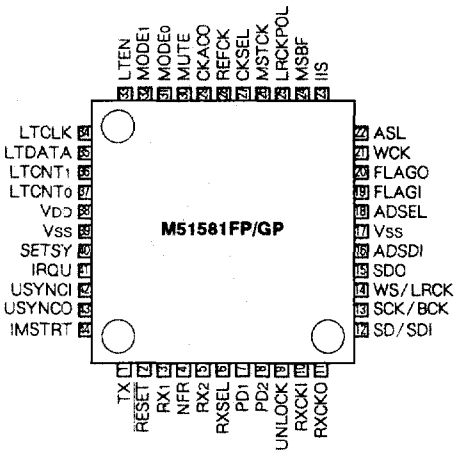
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{DD} = 4.5 to 5.5V
Rated supply voltage ..... V_{DD} = 5V

SYSTEM CONFIGURATION

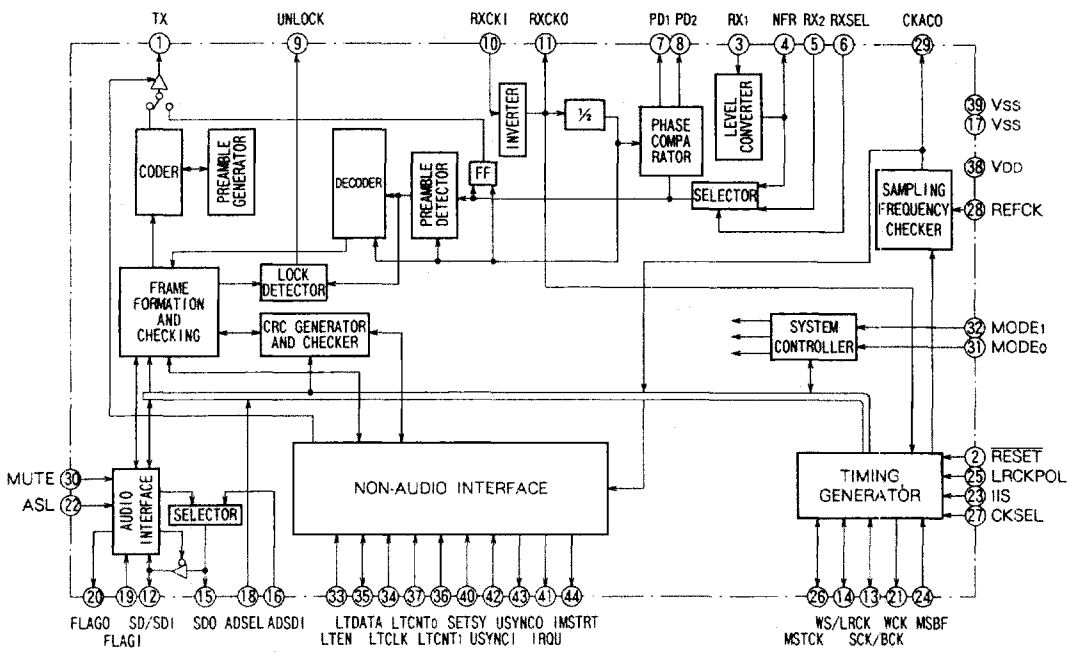


PIN CONFIGURATION (TOP VIEW)



Outline 44P6W-B(FP)
44P6N-A(GP)

IC INTERNAL BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTION

COMMON PINS (O"and Bi denote tri-state output and bi-directional transmission, respectively.)

Pin No.	Name	I/O	Function
①	TX	O"	Digital audio data output in EIAJ format
②	$\overline{\text{RESET}}$	I	Reset : "0" = reset (in microcomputer mode : fs = 48kHz, TX disabled)
③	RX_1	I	Digital audio data input 1 in EIAJ format : for input via coaxial cable(200mVp-p min.)
④	NFR	O	RX_1 level converter output (Connect a feedback resistor.)
⑤	RX_2	I	Digital audio data input 2 in EIAJ format : for input via optical cable(CMOS level)
⑥	RXSEL	I	RX input selection : "1" = RX_1 ; "0" = RX_2. In microcomputer mode, this pin is for selecting the polarity of RXSEL
⑦	PD_1	O	Output of phase detector for charge pump VCO
⑧	PD_2	O	
⑨	UNLOCK	O	Output of unlock detector : "1" = unlock
⑩	RXCKI	I	VCO clock input (256fs)
⑪	RXCKO	O	VCO clock output ($\overline{\text{RXCKI}}$)
⑫	SD/SDI	Bi/I	Serial audio data input/output (input only except for I^2S format)
⑬	SCK/BCK	Bi	Audio data bit clock input/output
⑭	WS/LRCK	Bi	Audio data word select input/output
⑮	SDO	O	Serial audio data output
⑯	ADSDI	I	Serial audio data input from AD converter
⑰	V_{SS}	–	Ground
⑱	ADSEL	I	Serial audio data source selection : "1" = analog (AD converter) ; "0" = digital (RX) ; in microcomputer mode, this pin is for selecting the polarity of ADSEL
⑲	FLAGI	I	Error flag input
⑳	FLAGO	O	Error flag output
㉑	WCK	O"	Word clock output (2fs at reception)
㉒	ASL	I	Audio data sampling length selection : "1" = 24 bits ; "0" = 16 bits
㉓	IIS	I	Audio data format selection : "1" = I^2S ; "0" = Any other format than I^2S
㉔	MSBF	I	MSB selection : "1" = MSB first ; "0" = LSB first
㉕	LRCKPOL	I	LRCK polarity selection : "1" = Lch→1 ; "0" = Lch→0
㉖	MSTCK	Bi	Master clock input/output (128fs or 256fs)
㉗	CKSEL	I	Master clock frequency selection : "0" = 256fs ; "1" = 128fs
㉘	REFCK	I	Reference clock input for checking the accuracy of sampling frequency (9.408MHz)
㉙	CKACO	O	Checking result output of the accuracy of sampling frequency : "1" = ± 0.14% or more of frequency error
㉚	MUTE	I	Mute control : "1" = mute ; In microcomputer mode, this pin is for selecting the polarity of mute control
㉛	$MODE_0$	I	Mode selection : ($MODE_1$, $MODE_0$) "0, 0" = microcomputer mode "0, 1" = easy mode "1, 0" = full-transparent mode "1, 1" = test mode
㉜	$MODE_1$	I	
㉞	V_{DD}	–	Power supply
㉟	V_{SS}	–	Ground

EASY MODE (PROFFESIONAL), (at ㊵pin "TYPE"="1")

Pin No.	Name	I/O	Function
㉝	IN/OUT	I	Transmission selection : "1" = receive ; "0" = transmit
㉞	PSL	Bi	Professional audio data sampling length selection:"1"=24 bits; "0"=20 bits
㉟	CRCO	O	CRC checking result output : "1" = error
㊱	TXOE	I	TX output enable : "1" = enable
㊲	FSINSEL	I	fs information selection(in reception) : "0" = fs information on C-bits, "1" = detected fs
㊵	TYPE	Bi	Type information "1" = Type I (professional = "1")
㊶	FS_O	Bi	fs information (in transmission : input) / fs information (in reception : output)
㊷	FS_1	Bi	(FS_O, FS_1) "0, 0" = 48kHz default, "0, 1" = 48kHz, "1, 0" = 44.1kHz, "1, 1" = 32kHz / fs information on C-bits(FSINSEL = "0"): "0, 0"=48kHz default, "0, 1"=48kHz, "1, 0"=44.1kHz, "1, 1"=32kHz / Detected fs (FSINSEL = "1"): 44.1kHz = "0, 0", 48kHz = "1, 0", 32kHz = "1, 1"
㊸	PLOCK	Bi	Source lock information : "1" = unlock
㊹	EMP	Bi	Emphasis information : "1" = 50μ/15μsec

EASY MODE (CONSUMER), (at ㊵pin "TYPE"="0")

Pin No.	Name	I/O	Function
㉝	IN/OUT	I	Transmission selection : "1" = receive ; "0" = transmit
㉞	CAT_O	Bi	Category information : (CAT_1, CAT_O) "0, 0" = general, "0, 1" = CD, "1, 0" = BS, "1, 1" = DAT
㉟	CAT_1	Bi	
㊱	TXOE	I	TX output enable : "1" = enable ; "0" = disable (high impedance)
㊲	FSINSEL	I	fs information selection(in reception) : "0" = fs information on C-bits ; "1" = detected fs
㊵	TYPE	Bi	Type information : "0" = Type II (consumer = "0")
㊶	FS_O	Bi	fs information (in transmission : input) / fs information (in reception)
㊷	FS_1	Bi	(FS_O, FS_1) "0, 0" = 44.1kHz, "0, 1" = 48kHz, "1, 1" = 32kHz / fs information on C-bits(FSINSEL = "0"): "0, 0"=44.1kHz default, "0, 1"=48kHz, "1, 1"=32kHz / Detected fs (FSINSEL = "1"): 44.1kHz = "0, 0", 48kHz = "1, 0", 32kHz = "1, 1"
㊸	COPY	Bi	Copy information : "1" = enable
㊹	EMP	Bi	Emphasis information : "1" = 50μ/15μsec

MICROCOMPUTER MODE (LT BUS MODE)

Pin No.	Name	I/O	Function
㉞	LTEN	I	LT interface enable : "1" = enable
㉟	LTCLK	I	Bit clock input for LT interface data
㊱	LTDATA	Bi	LT interface data input/output
㊲	$LTCNT_1$	I	LT interface control : ($LTCNT_1$, $LTCNT_0$) "0, 0" = C-bit data "0, 1" = U-bit data "1, 0" = setting "1, 1" = status
㊳	$LTCNT_0$	I	
㊵	SETSY	I	Setting latch clock input
㊶	IRQU	O	U-bit data information message indicator output
㊷	USYNCI	I	U-bit data unit indicator input (in transmission)
㊸	USYNCO	O"	U-bit data unit indicator output (in reception)
㊹	IMSTRT	O	U-bit data message start indicator output

FULL-TRANSPARENT MODE

Pin No.	Name	I/O	Function
㉝	IN/OUT	I	Transmission selection : "1" = receive ; "0" = transmit
㉞	BKSYO	O	C-bit block sink output (preamble "B" detected)
㉟	CRCO	O	CRC check output : "1" = error
㊱	TXOE	I	TX output enable : "1" = enable
㊲	$DETFS_0$	O	Detected fs ($DETFS_0$, $DETFS_1$) 44.1kHz = "0, 0" 48kHz = "1, 0" 32kHz = "1, 1"
㊵	$DETFS_1$	O	
㊶	$CDAT_1$	I	C-bit data input
㊷	CDATO	O	C-bit data output
㊸	$UDAT_1$	I	U-bit data input
㊹	UDATO	O	U-bit data input

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage	−0.3	−	6.5	V
P_d	Power dissipation	−	−	600	mW
V_I	Input voltage	−0.3	−	V_{DD}+0.3	V
V_O	Output voltage	−0.3	−	V_{DD}+0.3	V
I_O	Output current	−	−	± 16	mA
T_{opr}	Operating temperature	−30	−	70	℃
T_{stg}	Storage temperature	−50	−	125	℃

RECOMMENDED OPERATING CONDITIONS (V_{DD} = 5V, Ta = − 30℃ to 70℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Supply voltage		4.5	5.0	5.5	V
V_{IL}	Input voltage ("L" level)	V_{DD} = 4.5V	0	−	1.35	V
V_{IH}	Input voltage ("H" level)	V_{DD} = 5.5	3.85	−	V_{DD}	V
t_{ri}	Input rise time		−	−	500	ns
t_{fi}	Input fall time		−	−	500	ns
L_I	Input leak current	V_I = 0, V_{DD}	−	−	± 1	μA
I_{OL}	Output current ("L" level)	V_{OL} = 0.4V, V_{DD} = 4.5V	14	−	−	mA
I_{OH}	Output current ("H" level)	V_{OH} = 4.1V, V_{DD} = 4.5V	−	−	− 5	mA
V_{OL}	Output voltage ("L" level)	I_{OL} < 1 μA	4.95	−	−	V
V_{OH}	Output voltage ("H" level)	I_{OH} < − 1 μA	−	−	0.05	V

All inputs are at CMOS level

FUNCTION DESCRIPTION

1. Reset conditions

(1) Reset action

(a) All setting bits are set to 0 (in microcomputer mode) Transmission mode ADSEL, TEST, BCKPOL, MUTE, RXSEL, TXOE, NOWD = 0

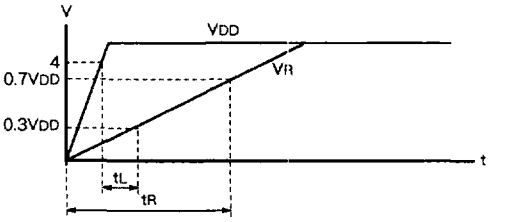
(b) The lock detector is initialized

(c) The sampling frequency accuracy checker is initialized

(2) Master clock

While resetting, the master clock should not necessarily be supplied. (It is also permissible to supply it.)

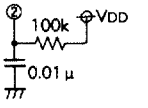
(3) Reset time



RECOMMENDED OPERATING CONDITIONS FOR RESETTING

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_L	L level hold time	V_{DD} > 4V to V_R < 0.3V_{DD}	50	−	−	μs
t_R	L level reset time	V_{DD} = 5V, CR = 100k/0.01 μ	−	1.2	−	ms

RECOMMENDED CIRCUIT



2. RECOMMENDED OPERATING CONDITIONS FOR RX1 INPUT VOLTAGE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IRX1}	RX1 input voltage	fs < 50kHz	200m	−	V_{DD}	V_{P-P}

MITSUBISHI ELECTRIC

3. Audio Interface

(1) Format I²S/non-I²S

(2) Number of significant bits 16bits/24bits

(3) Error flag

If one of the following conditions occurs in reception mode, an error flag is sent

- Validity flag = 1(error)
- Parity check result = 1(error)
- PLL does not lock

(4) Preceding-value holding

If the result of parity check is an error, the preceding value in audio data is held

(5) Mute

If PLL is unlocked in reception mode, the signal is muted automatically. In addition, it is possible to mute a signal compulsively with the MUTE pin

4. Non audio interface

Non audio data includes the following

- Channel status
- User data
- Settings (to set IC operating conditions)
- Status (Monitored IC operating conditions)

Control methods as shown below are available for non audio data

MODE00 – Microcomputer mode

In this mode the M51581FP is controlled by a microcomputer via LT bus by serial data

MODE01 – Easy mode

The M51581FP is controlled by means of dedicated pins

MODE10 – Full-transparent mode

In this mode a microcomputer is used to receive and process all bits of both C and U bits

5. Checking the accuracy of sampling frequency

It is possible by means of the sampling frequency checker to check whether received signals are within approximately ±0.14% of the reference value. With this checking function, recorded patterns on a DAT tape and the like are prevented from shifting. It is also possible to judge to which range of the three reference values (32k, 44.1k, or 48kHz) the sampling frequency of the received signal correspond (fs detection function). If these functions, sampling frequency accuracy check and fs detection, are not used, pin㉘ REFCK does not require the reference clock.

Fix pin㉘ to L in that case.

6. PLL lock detection

In the following conditions, PLL is judged to be unlocked

- No preamble has been detected
- Parity check resulted in two consecutive errors

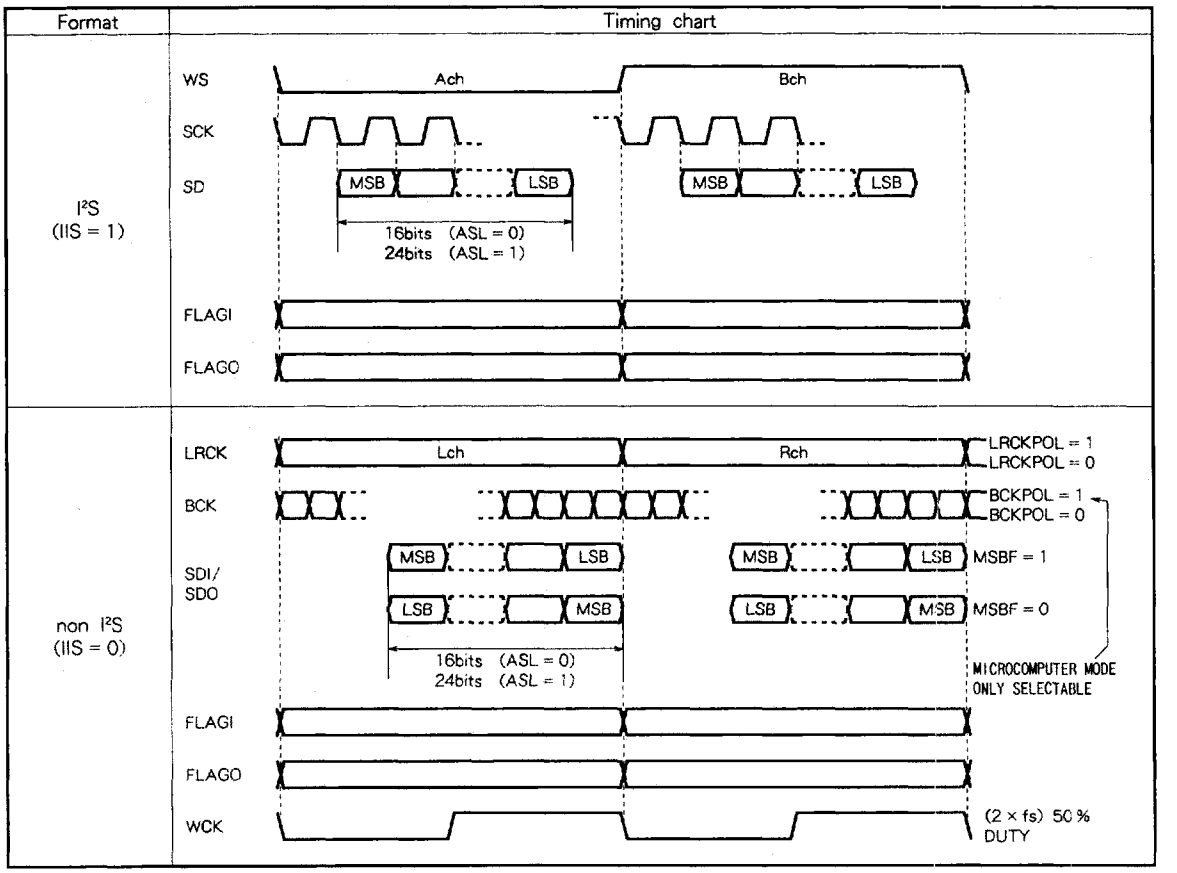
TIMING CHART

1. AUDIO INTERFACE FORMAT

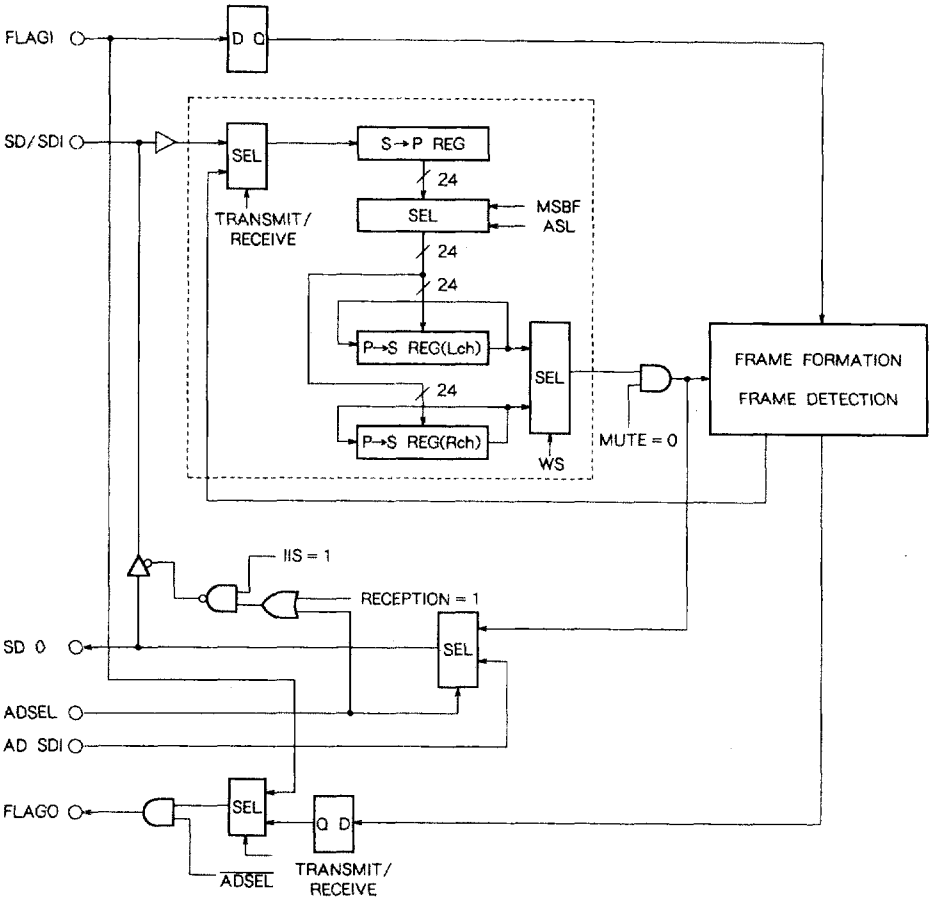
(1) Audio interface format conditions

Selection pin			Format	Audio data	WS/LRCK
IIS	MSBF	LRCKPOL			
1	1	0	I²S	MSB first 16bits (ASL = 0) 24bits (ASL = 1)	Ach = 0 Bch = 1
0	1	0	non-I²S	↑	Lch = 0 Rch = 1
	1	1		↑	Lch = 1 Rch = 0
	0	0		LSB first 16bits (ASL = 0) 24bits (ASL = 1)	Lch = 0 Rch = 1
	0	1		↑	Lch = 1 Rch = 0

(2) Audio interface format timing chart



(3) Audio interface block diagram



(4) Operation status of FLAGO, SD/SDI

			I^2S		non-I^2S	
DAT operation mode	DAI transmission	ADSEL	FLAGO	SD/SDI	FLAGO	SD/SDI
Reproduction	Transmit	"0"	FLAGI	Input	FLAGI	Input
Analog recording	Transmit	"1"	"0"	Output (ADSDI)	"0"	Input
Digital recording	Receive	"0"	Data on received V bits	Output (received data)	Data on received V bits	Input

2. MICROCOMPUTER MODE DATA FORMAT

(1) LTDATA selection

Signal name			Data contents of LTDATA
LTEN	$LTCNT_1$	$LTCNT_0$	
1	0	0	C-bit data
1	0	1	U-bit data
1	1	0	Setting (microcomputer → DAI)
1	1	1	Status (DAI → microcomputer)

(2) Settings (8-bit)

1	2	3	4	5	6	7	8

Bit	Function
1	Transmission selection : "1" = receive, "0" = transmit
2	ADSEL : Serial audio data source selection ; Polarity is determined by ADSEL (pin 18).(Note 1)
3	Test : Fixed to "0" normally
4	BCKPOL:Bit clock(BCK)polarity selection; If this bit is "0," BCK falls at LRCK edges
5	MUTE : Mute control ; Polarity is determined by MUTE(pin 30).(Note 1)
6	RXSEL:RX input selection;Polarity is determined by RXSEL(pin 6)(Note 1)
7	TXOE : TX output enable ; "1" = enable
8	NOWD : Timing control for USYNCI and USYNCO ; "0" = no delay "1" = 4WS delay

(3) Status (8-bit) (8-bit)

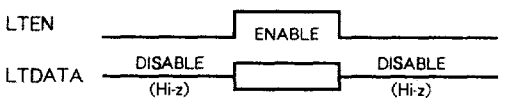
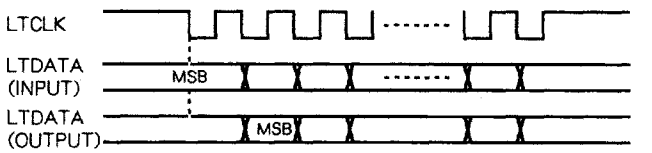
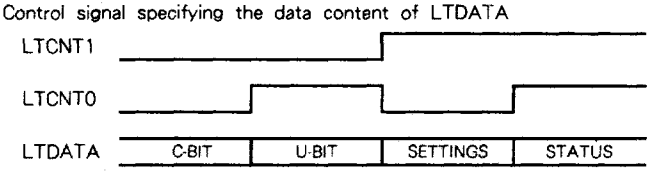
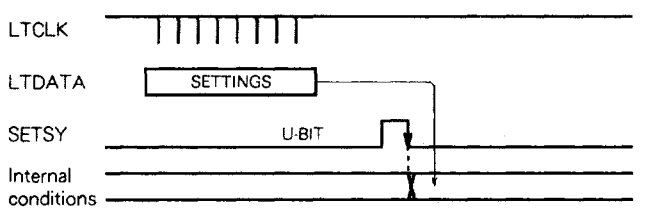
1	2	3	4	5	6	7	8

Bit	Function
1	UNLOCK : PLL unlock information ; "1" = unlock
2	CKACO : Output sampling frequency accuracy check ; "1" = frequency error greater than ± 0.14 %
3	DETFS0 ⎫ Detected fs (DETFS0, DETFS1) 44.1kHz = "0, 0" 48kHz = "1, 0" 32kHz = "1, 1"
4	DETFS1 ⎭

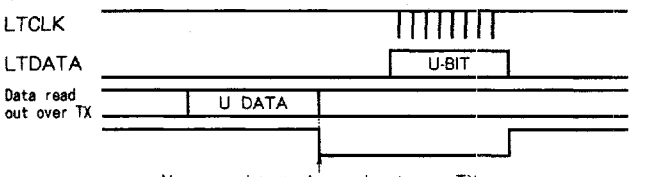
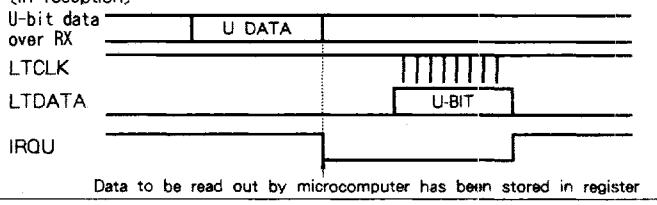
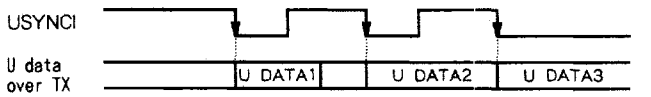
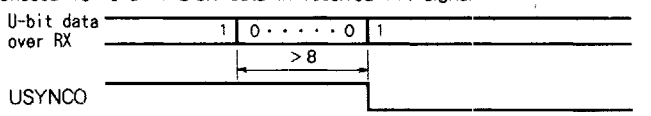
(Note 1) In microcomputer mode, functions listed below are determined by the polarity of both the dedicated pins and setting bits.

Name	Function	Polarity of dedicated pins		Polarity of setting bits	
ADSEL	Serial audio data source selection	ADSEL ⑱ pin	"0"	Bit 2	"1" = analog, "0" = digital
			"1"		"0" = analog, "1" = digital
MUTE	Mute control	MUTE ㉚ pin	"0"	Bit 5	"1" = mute
			"1"		"0" = mute
RXSEL	RX input selection	RXSEL ⑥ pin	"0"	Bit 6	"1" = RX1, "0" = RX2
			"1"		"0" = RX1, "1" = RX2

PIN DESCRIPTION (Microcomputer mode, pins for LT bus)

Pin No.	Name	I/O	Function and timing
㉝	LTEN	I	Enable control signal for LTDATA  When LTEN = 0, the input to LTDATA is enabled while LTCLK is disabled This is used as a selection signal for parallel connection to another system via LT bus
㉞	LTCLK	I	Clock input for shift-in and shift-out of LTDATA Although 8 or 16 clock pulses are handled as a unit, it is permitted to stop at smaller clock pulses if performing mode change by LTCNT0 and LTCNT1 which resets LTCLK
㉟	LTDATA	I/O	Serial data input/output  In data input state, data is taken into the IC at the positive-going edge of LTCLK. In data output state, the first bit is delayed by approximately 100ns at the maximum from the negative-going edge of LTCLK. The second and later bits are shifted out at the negative-going edge of LTCLK Whether to input or output data depends on the mode determined by LTCNT0 and LTCNT1 and on whether the action is to transmit or receive
㊱ ㊲	LTCNT1 LTCNT0	I I	Control signal specifying the data content of LTDATA  Settings : Sets the internal conditions of the IC (transmit/receive, etc.) Status : Monitors the internal conditions of the IC (unlock, etc.) Internal counters and the like are reset at either edge of both signals
㊵	SETSY	I	Latch clock input for settings information sent by LTDATA 

PIN DISCRIPTIONS (Continue)

Pin No.	Name	I/O	Function and timing
㊶	IRQU	O	Output signal specifying the state of the internal register that is the buffer for inputting and outputting U-bit data 〔In transmission〕  No more data to be read out over TX 〔In reception〕  Data to be read out by microcomputer has been stored in register
㊷	USYNCI	I	Control signal specifying during transmission the timing to read out over TX U data consisting of units of 8 bits and stored in the internal register  Two kinds of timing are available to choose from by means of NOWD in settings data If NOWD = 0, timing is at the negative or positive-going edge of USYNCI with no time delay If NOWD = 1, U-bit data is transmitted at the position 4 fs words after each negative-going edge of USYNCI
㊸	USYNCO	O	Signal output indicating during reception word sink, namely, 9 bits or more consecutive "0"s in U-bit data in received RX signal  Two kinds of timing are available to choose from by means of NOWD as is in the case of USYNCI If NOWD = 0, USYNCO is inverted each time word sink occurs without delay If NOWD = 1, USYNCO is set to "0" after a time delay of 4 fs words from word sink, then set to "1" 2 fs words thereafter
㊹	IMSTRT	O	This signal during reception also indicates word sink similarly to USYNCO. It is output in synchronization with the reading out from LTDATA of 8-bit data preceding word sink During transmission, it is an output signal indicating an occurrence of 9-bits or more consective "0"s in U-bit data read out over TX

• The timing of settings data

Eight-bit settings data inputted through LTDATA is latched by the internal register at the negative-going edge of SETSY and establishes IC operating conditions.

• The timing of status data

Internal operating conditions (PLL lock, etc.) are loaded into the shift register at the negative-going edge of the first bit of LTCLK. They are shifted out bit by bit at the following negative-going edges.

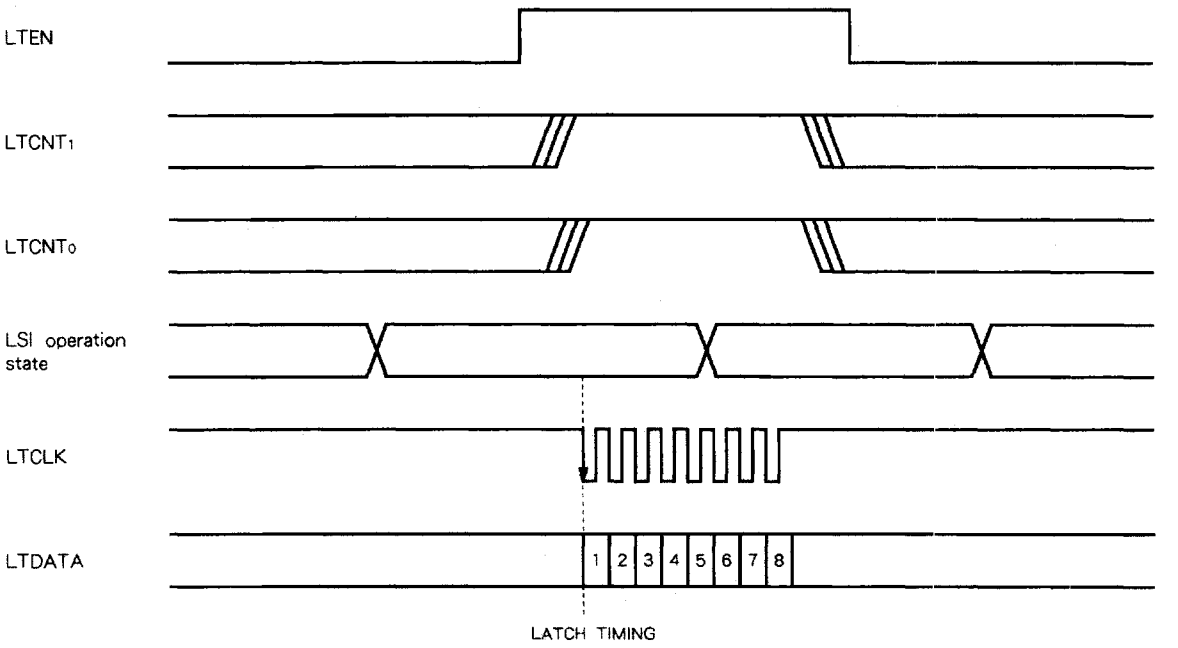
• The timing of C bit

Channel status can be inputted to and output from a block (192 frames) in units of 16 bit. In order for C bit during transmission to be sent over TX in such a manner that another data set is contained in another block, 16 bit of C-bit data entering the IC will be sent over TX at the beginning (the position of preamble "B") of the next block. Regarding 16 bit of data inputted as LTDATA, they will move to other latches within approximately 500ns after the 16th bit has entered, so that the next 16 bit of data can be successively inputted to the IC.

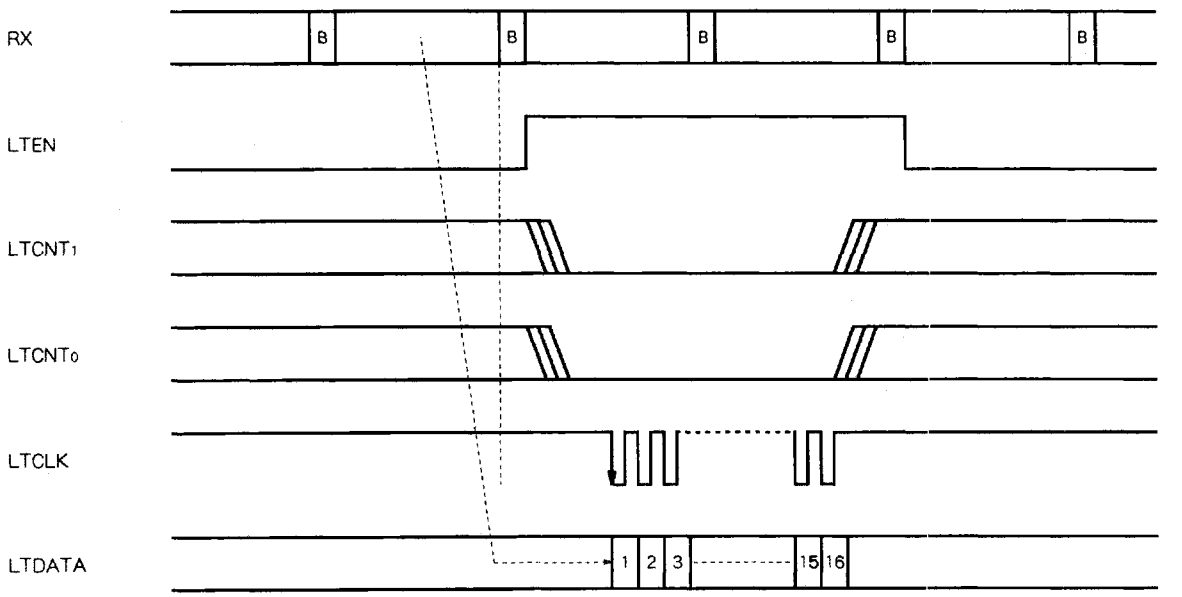
The 16 C bit contained in the previous block and held in internal latches during reception are loaded to the shift register in parallel form at the negative-going edge the first bit of LTCLK. They will be shifted out at the next negative-going edge of LTCLK.

3. DATA READ OUT TIMING (DAI→MICROCOMPUTER)

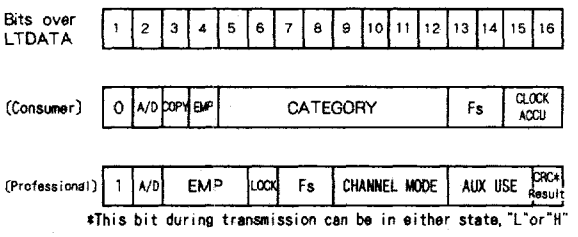
(1) Status



(2) C-bit data (reception mode)



Contents of C-bit data



(3) U-bit data (reception mode)

1) The general form of U-bit data

The general form is suitable for the U-bit data of CD and DAT. In that form as shown in Fig. 1 one unit of U-bit data consists of 8 bits, namely, a sink bit (= 1) at the beginning plus following 7 information bits.

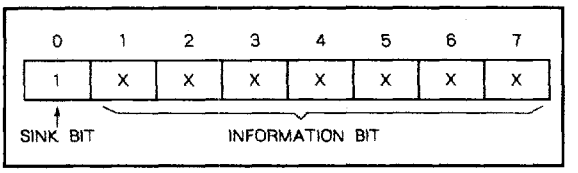


Fig. 1 U-bit data unit structure

Any number of "0"s can be inserted between units during transmission as shown in Fig. 2 If 9 or more "0"s are inserted in succession, the following unit is the start of a message. In other words, more than one units constitute a message and 9 or more "0"s separate messages.

The M51581FP in microcomputer mode is designed to interface in accordance as a rule with the general form of U-bit data.

At the reception block in particular, data is processed unit by unit assuming that U-bit data in received signals is conforming to the general form.

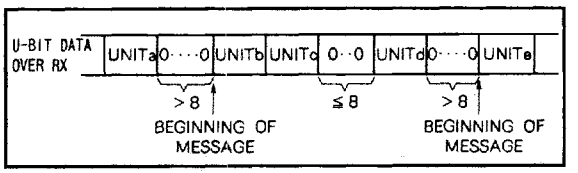


Fig. 2 The general transmission form of U-bit data

2) The structure of the U-bit data registers

The U-bit data registers are 4 pieces of byte registers (8 bits), an outline of which is shown in Fig. 3 Each register has independent addresses for writing and reading data. Data is written according to LTCLK given by a microcomputer. When 8 bits of data are written, the writing address increases by one. On the other hand, data is read based on MSTCK. In reading, one bit is allocated to a subframe in U-bit data sent over TX. When one byte of data is read, the reading address increases by one. The 4 registers are used cyclically as they are counted up.

The timing to read the first bit stored in a register is decided by the USYNCI signal.

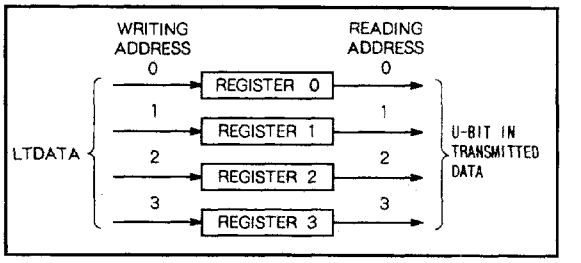


Fig. 3 The structure of U-bit data registers

3) U-Bit data timing during reception

The byte registers during reception are configured in the same way as transmission. Data is written and read based on MSTCK and LTCLK, respectively.

Received U-bit data is stored in the byte registers by information units. IRQU becomes "1" if read/write addresses coincide. This means, if IRQU is "0" new data received is written and is readable by microcomputer.

IMSTRT is "1" during the time between the start of reading the beginning unit of a message and the start of reading the next information unit. Consequently, a microcomputer during reception monitors IMSTRT, or USYNCO, which is explained later, to recognize the beginning of a message and also monitors IRQU to obtain U-bit data through LTDATA by LTCLK.

4) The Timing of USYNCI, USYNCO

As each subframe contains one U-bit, there is a U-bit in every 1/2 period of the LRCK signal. In applications of the IC to R-DAT especially, transmission should be managed so that audio sampling position during one drum turn coincides a U-bit. Since the U-bit read out position is based on USYNCI as explained above, inputting the drum revolution reference signal from the signal processing IC to USYNCI satisfies the requirements for R-DAT.

However, the frequency of the reference signal and the relationship between the positions of the reference signal and audio sampling are not uniform. For this reason, the M51581FP has two modes, which can be selected by NOWD in settings data. The two modes are defined as follows.

(In transmission)

NOWD = 0

- U-bit are read at both edges of USYNCI
- Reading U-bit starts 1/2 LRCK after an edge of USYNCI

NOWD = 1

- U-bit are read at the negative-going edges of USYNCI
- Reading U-bit starts 9/2 LRCK after a negative-going edge of USYNCI

(In reception)

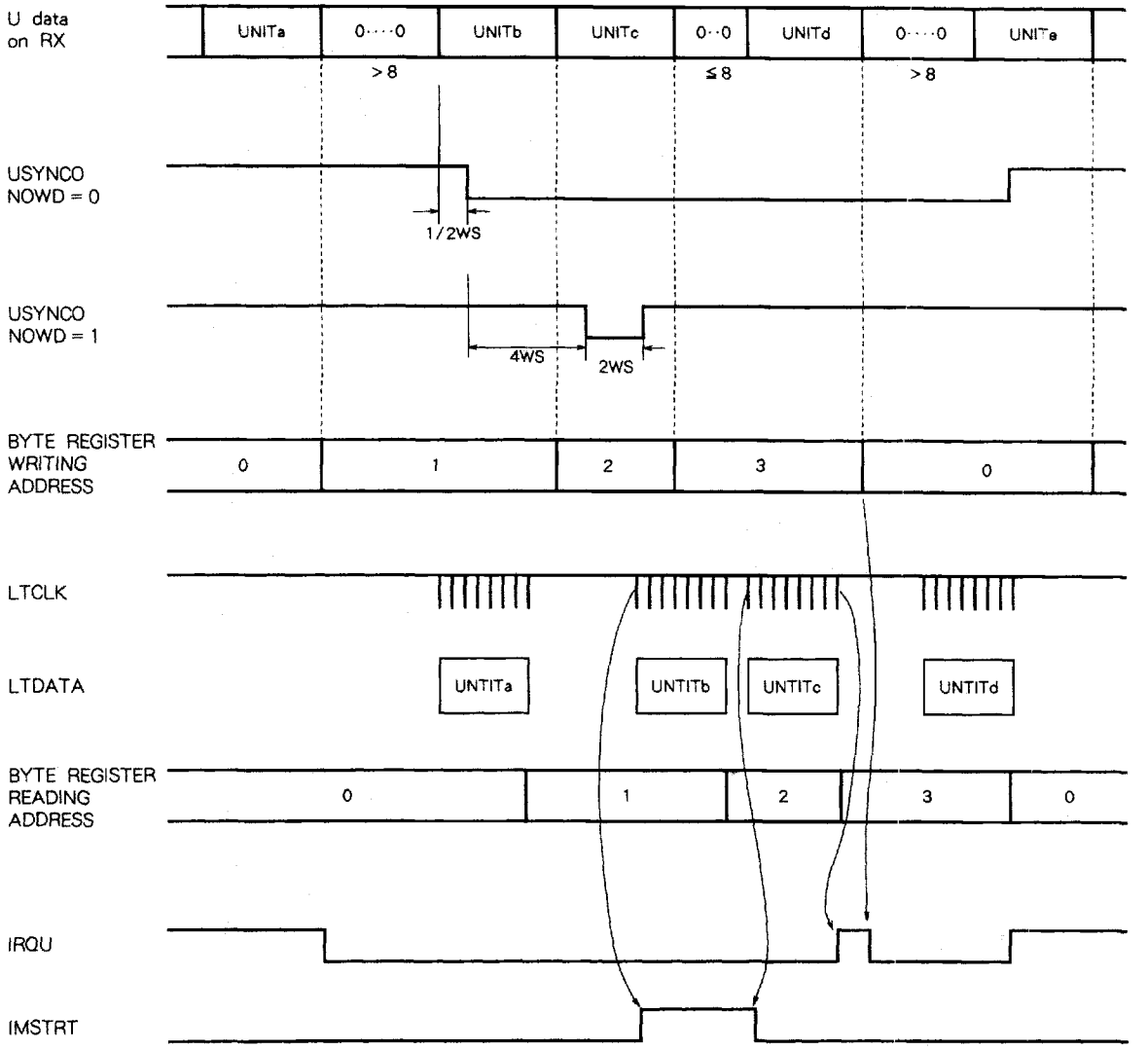
NOWD = 0

- The USYNCO signal is inverted at the beginning of each message
- USYNCO changes at an edge of LRCK following the sink bit of the beginning of a message

NOWD = 1

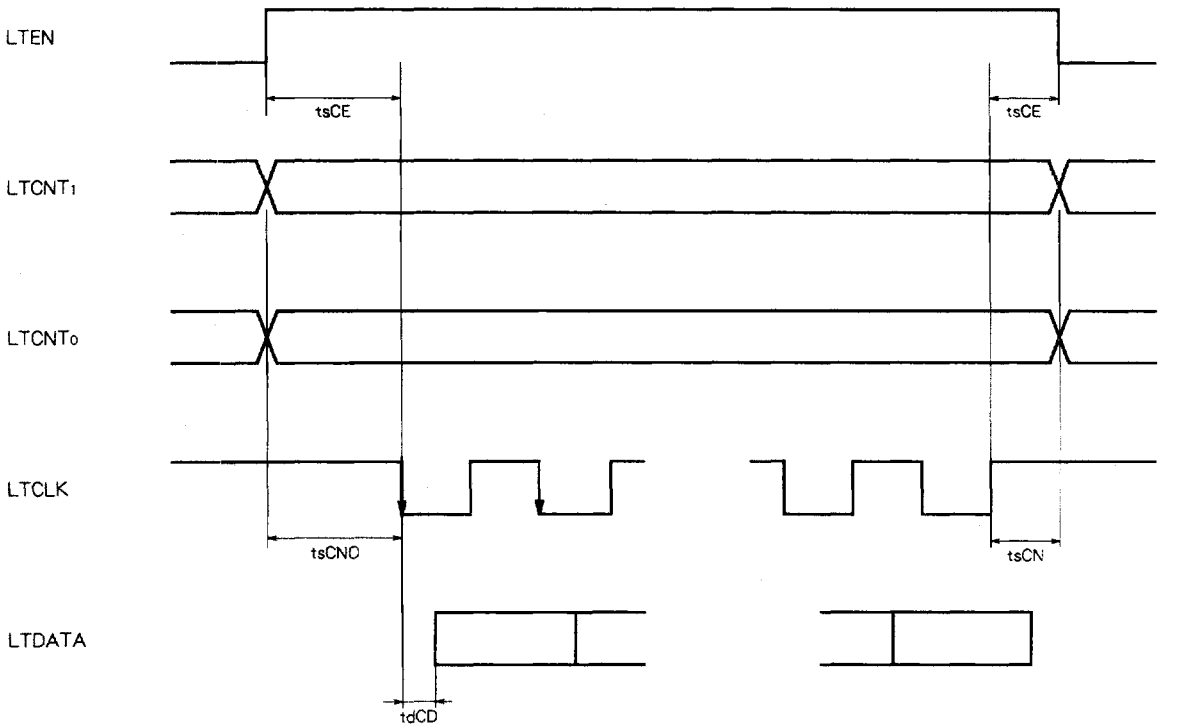
- USYNCO falls at an edge 4 LRCK after the sink bit of the beginning of a message
- USYNCO stays at "0" for a period of 2 LRCK

(4) U-bit data read out timing



(5) Timing limits for reading status, C-bit data, and U-bit data

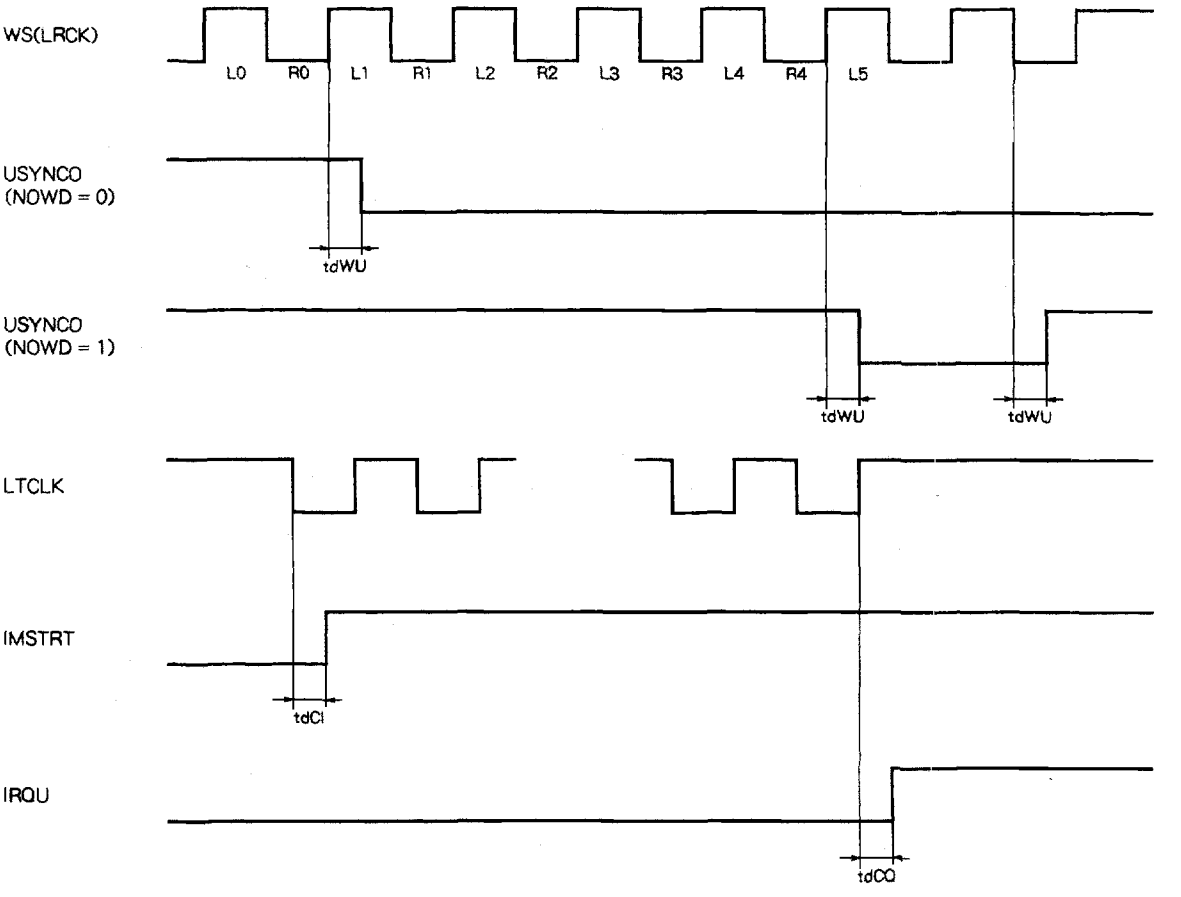
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
tsCEO	Data output LTCLK-LTEN setup time	1000			nsec
tsCE	LTCLK-LTEN setup time	50			nsec
tsCNO	Data output LTCLK-LTCNT setup time	1000			nsec
tsCN	LTCLK-LTCNT setup time	50			nsec
tdCD	LTCLK-LTDATA delay time			250	nsec



Note : As internal registers for data output are set at edges of the LTEN, LTCNT0, and LTCNT1 signals, at least one of these signals must be inverted in advance to read out status, C-bit data, and U-bit data.

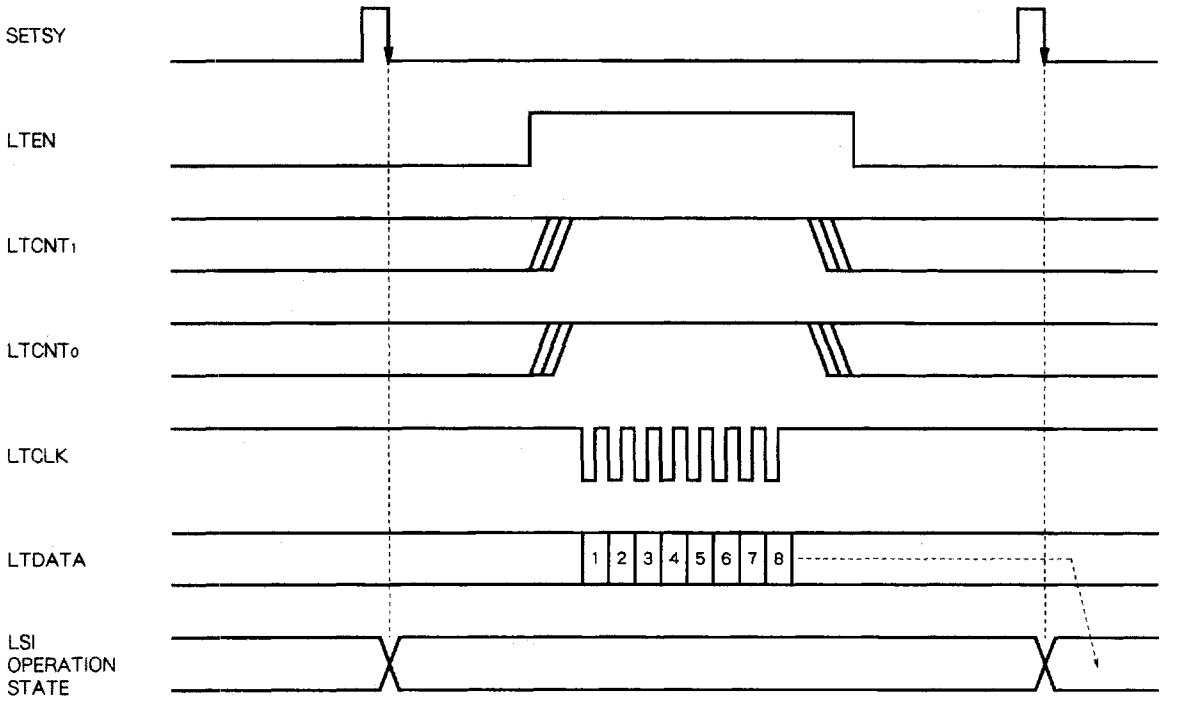
(6) Timing limits of usynco, IRQU, and IMSTRT

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
tdWU	WS-USYNCO delay time			200	nsec
tdCI	LTCLK-IMSTRT delay time			150	nsec
tdCQ	LTCLK-IRQU delay time			150	nsec

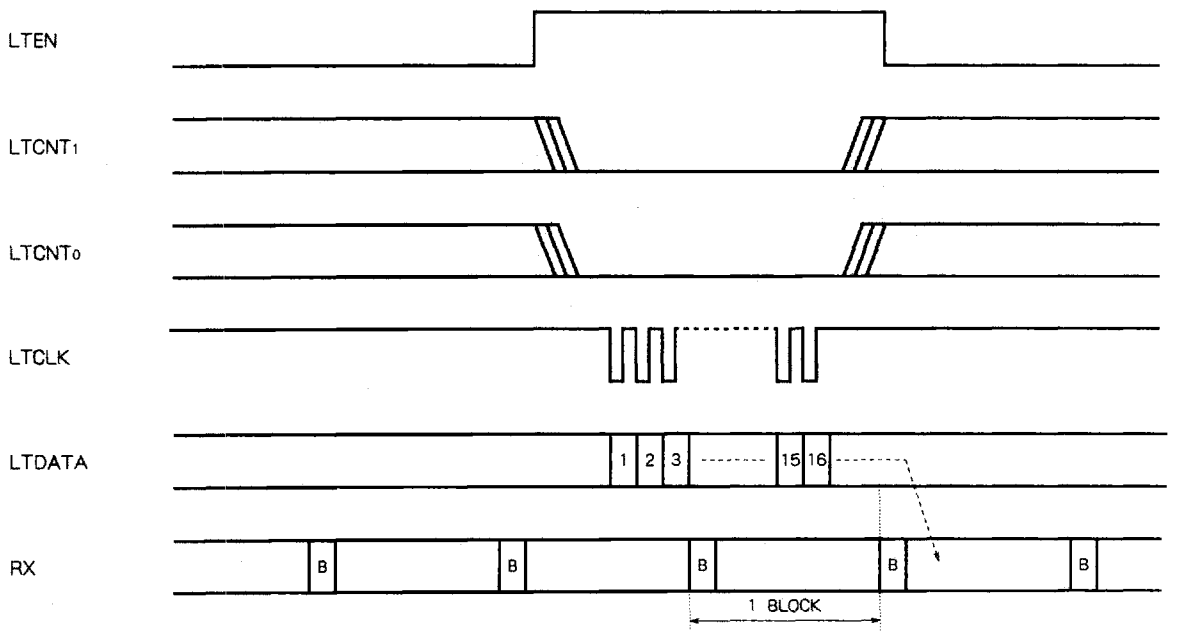


4. DATA WRITING TIMING (MICROCOMPUTER → DAI)

(1) Setting



(2) C-bit data (transmission mode)



(3) U-bit data (transmission mode)

Reading and writing the U-bit data registers are carried out in asynchronization with each other so that IRQU is used as a signal to recognize the state of the two addresses. If both addresses match, IRQU becomes "0". Since there is no more data to be transmitted (read) at this point, priority is given to writing, as a rule.

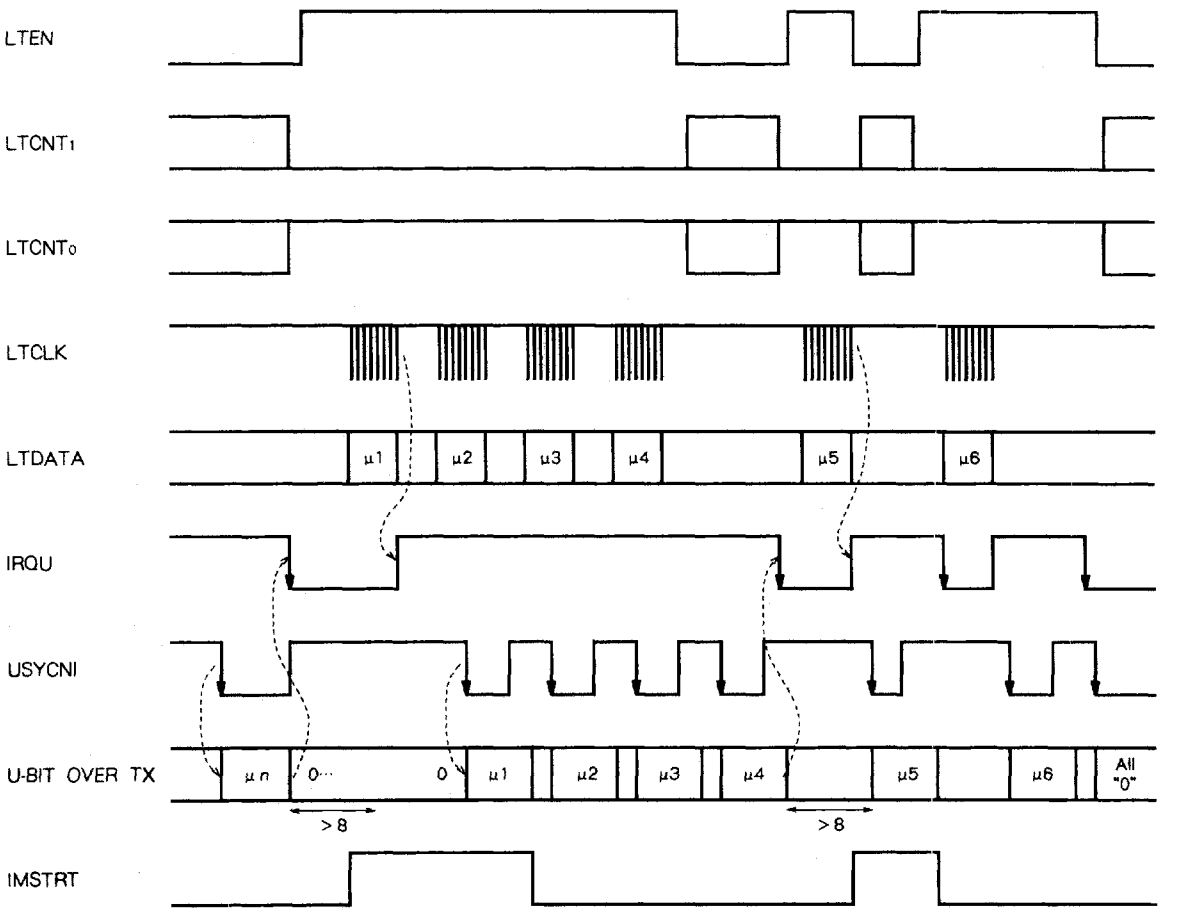
If IRQU = 0 and USYNCI falls (when NOWD = 1), transmission data will be all "0".

IMSTRT is a signal that if 9 or more continuous "0"s are found in U-bit data transmitted over TX stays at "1" until the end of reading the next 1 byte data.

As data is read based on USYNCI, a gap over 9-bit or more in USYNCI lets "0"s be transmitted as data on and after the 9th bit.

As explained above, the microcomputer, while monitoring IRQU, sends U-bit data to LTDATA by LTCLK. Furthermore, it can send U-bit at any desired positions by controlling USYNCI.

The M51581FP has 4 bytes of internal registers, so it is also possible to input 4 bytes of U-bit consecutively and then transmit them other TX by controlling USYNCI.



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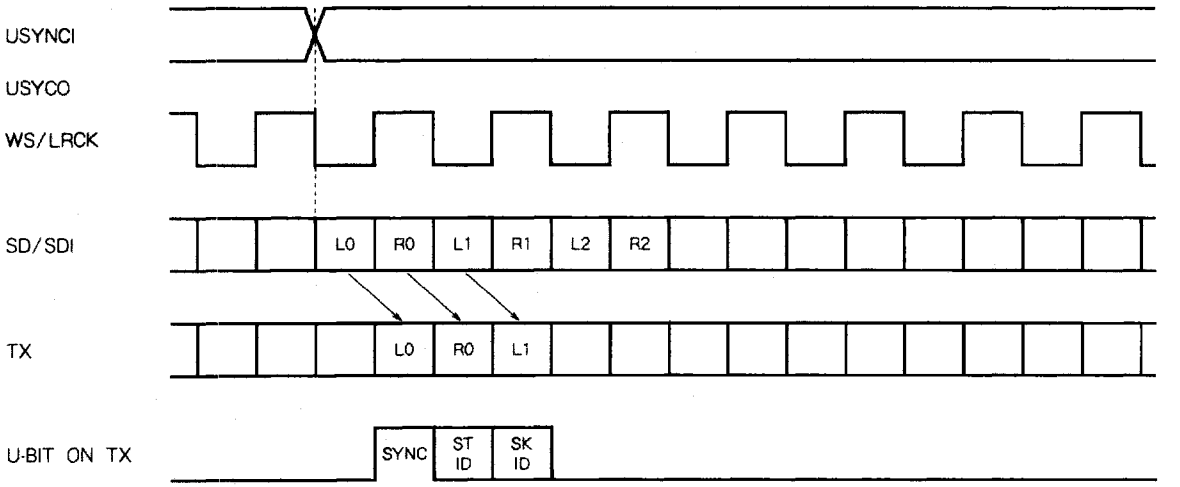
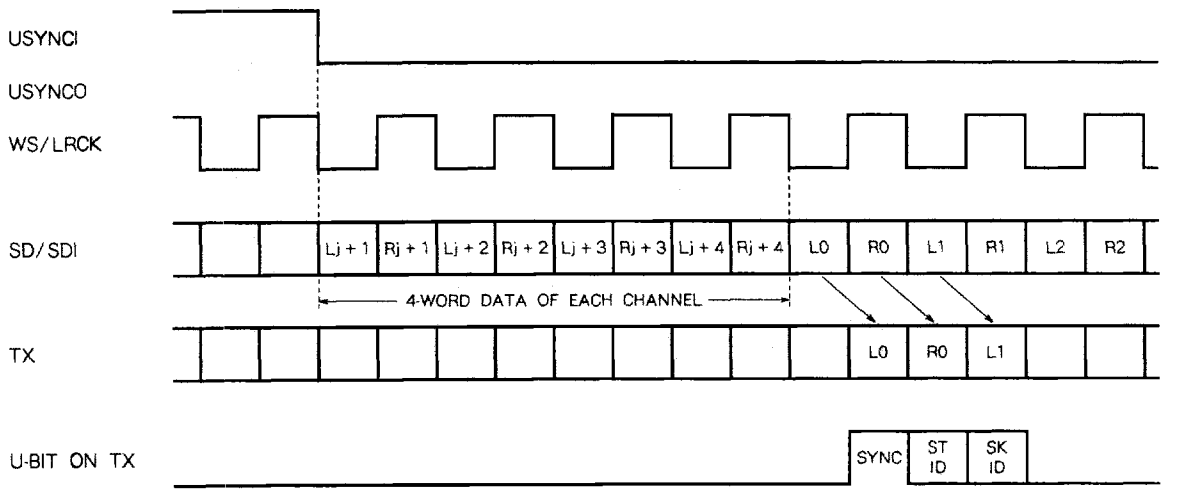
(4) The timing of USYNCI

(a) NOWD = 0

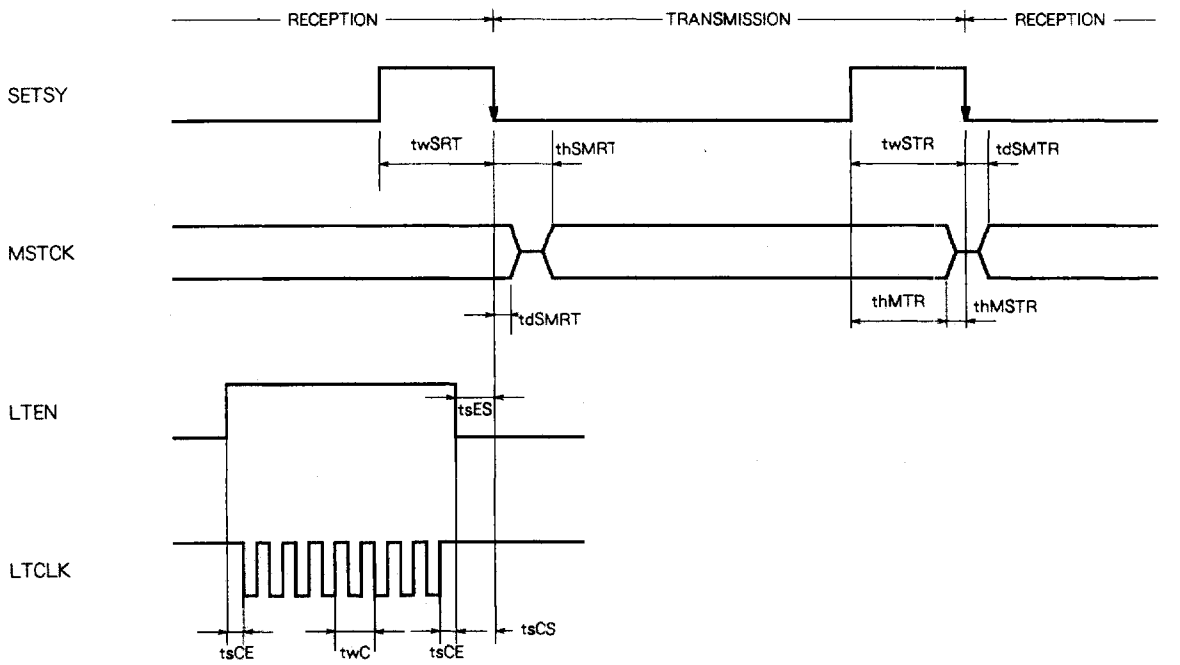


(b) NOWD = 1



(5) Setting timing limits

Symbol	Parameter	Limits (Unit : sec)			Remark
		Min	Typ	Max	
twSRT	SETSY pulse width at change from R to T	4μ	–	–	Value with an allowance considering the requirement of 4 clock pulses of MSTCK(128fs) in SETCY pulses and a failure of low VCO oscillation frequency
twSTR	SETSY pulse width at change from T to R	1μ	–	–	4 clock pulses under condition of fs = 32kHz assuming that MSTCK is stably supplied during transmission
thMTR	MSTCK hold time at change from T to R	1μ	–	–	4 clock pulses or more of MSTCK (128fs) in SETSY pulses meet the requirement
tdSMRT	SETS – MSTCK delay time at change from R to T	5n	30n	100n	Period taken by the MSTCK pin to shift from output mode to input mode (HI-z)
thMSTR	MSTCK – SETSY hold time at change from T to R	0n	–	–	Value with allowance to avoid interference between MSTCK outputs
thSMRT	SETSY – MSTCK hold time at change from R to T	100n	–	–	
tdSMTR	SETSY – MSTCK delay time at change from T to R	5n	30n	100n	Period taken by the MSTCK pin to shift from input mode (HI-z) to output mode
tsES	LTEN–SETSY setup time	–	–	–	No specification LTEN may be at "H" when SETSY falls
twC	LTCLK clock period	250n	–	–	
tsCE	LTCLK–LTEN setup time	50n	–	–	
tsCS	LTCLK–SETSY setup time	50n	–	–	



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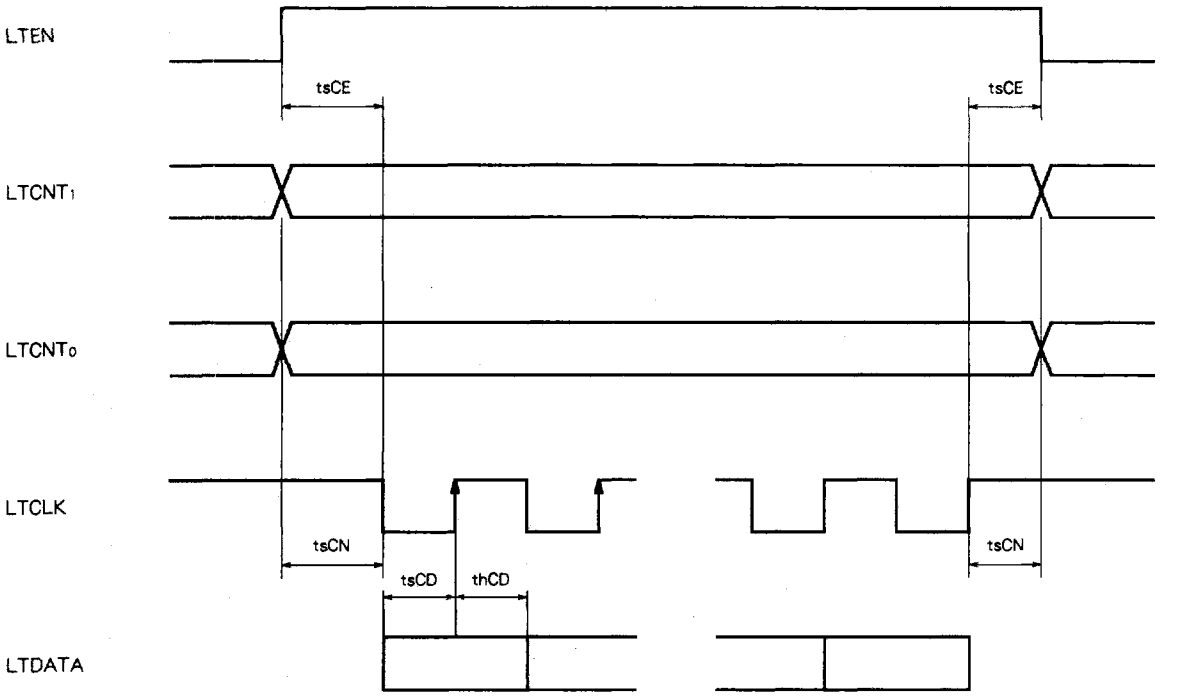
(6) Timing limits for writing settings, C-bit data, and U-bit data

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
tsCE	LTCLK–LTEN setup time	50			nsec
tcCN	LTCLK–LTCNT setup time	50			nsec
tsCD	LTCLK–LTDATA setup time	50			nsec
thCD	LTCLK–LTDATA hold time	50			nsec

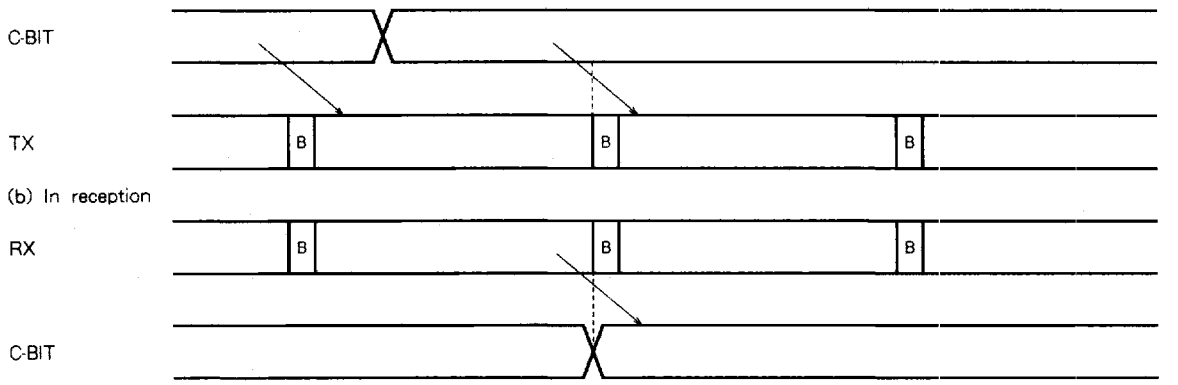


Note : As internal registers for data input are set at edges of the LTCNT0 and LTCNT1 signals, at least one of these signals must be inverted in advance to write settings, C-bit data, and U-bit data.

5. C-BIT DATA TIMING (EASY MODE)

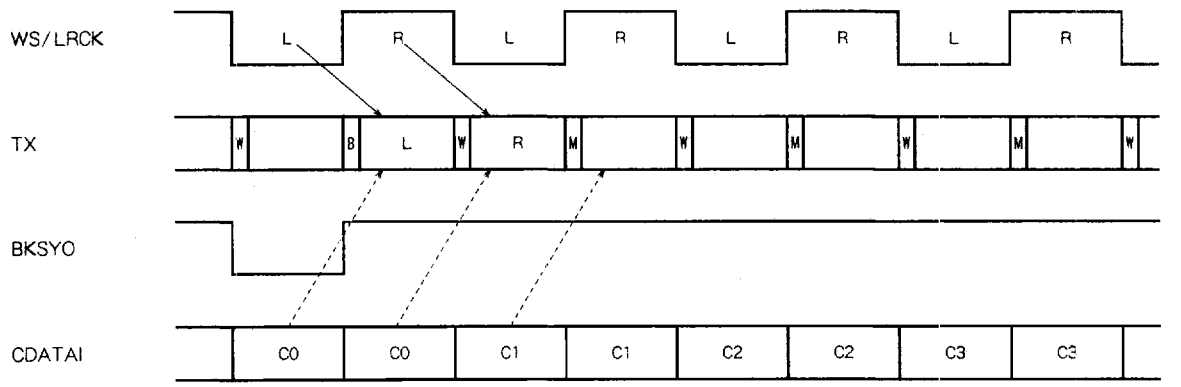
(1) C-bit data

(a) In transmission

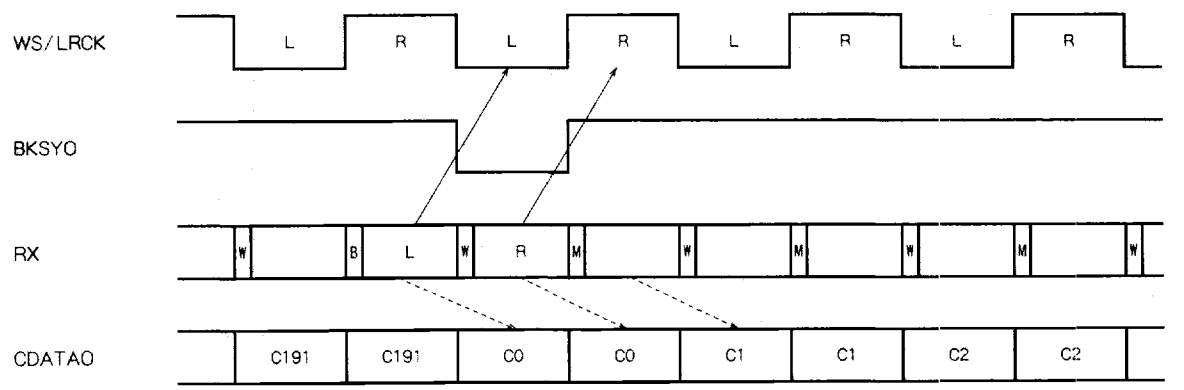


6. C-BIT DATA TIMING (FULL-TRANSPARENT MODE)

(a) In transmission



(b) In reception



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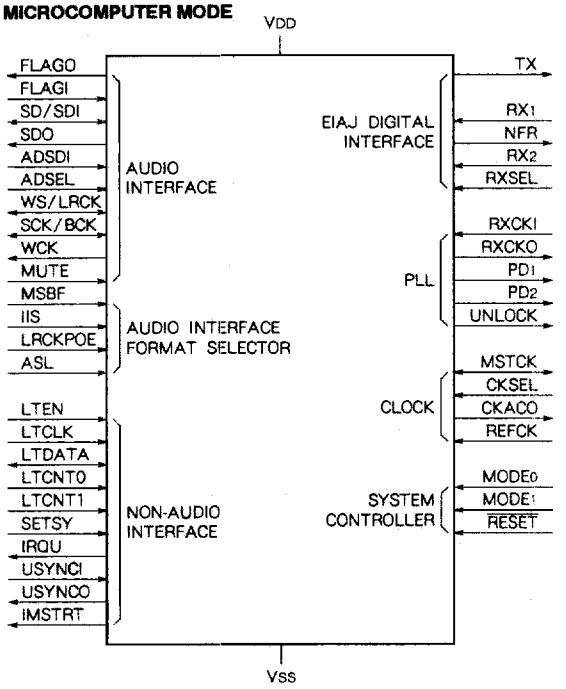
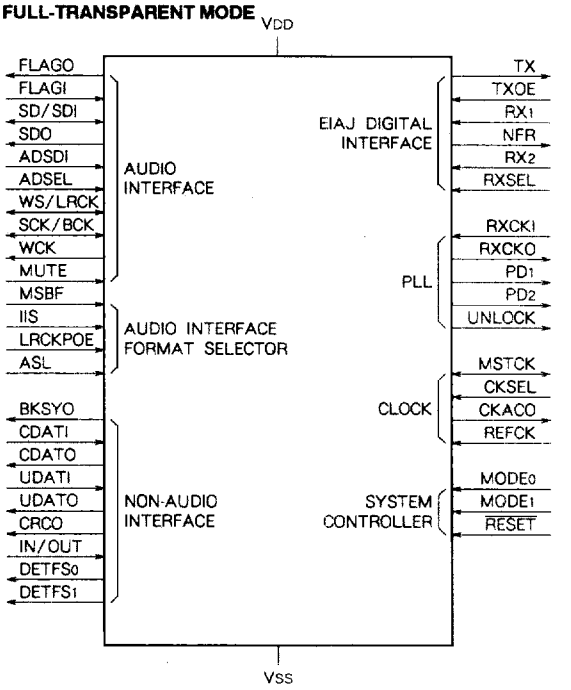
7. INPUT/OUTPUT PIN FORMAT

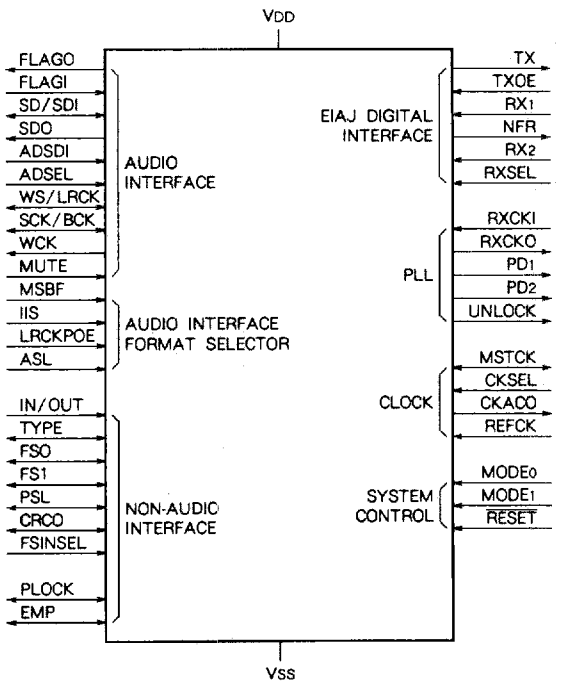
MICROCOMPUTER MODE



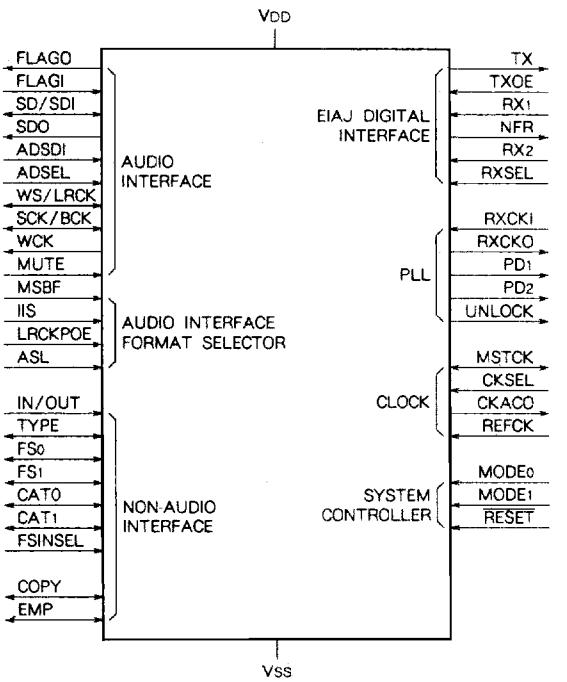
FULL-TRANSPARENT MODE



EASY MODE:PROFESSIONAL

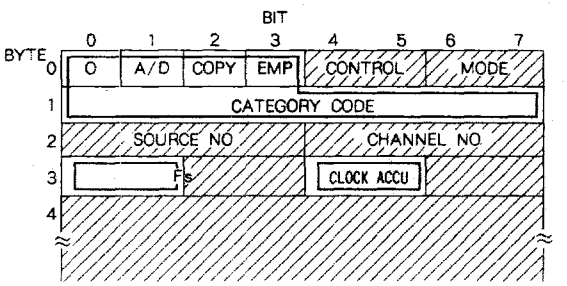


EASY MODE:CONSUMER

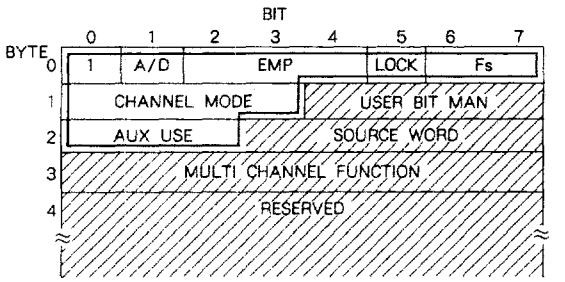


8. C-BIT DATA SUPPORT BIT MAP

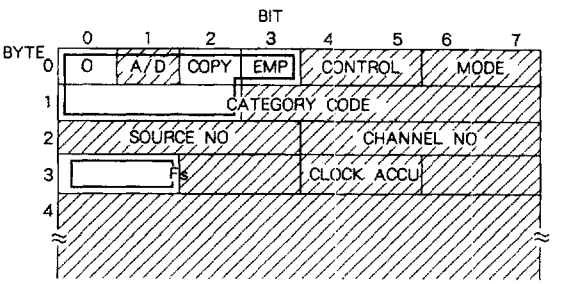
(1) Microcomputer (MODE00), Consumer



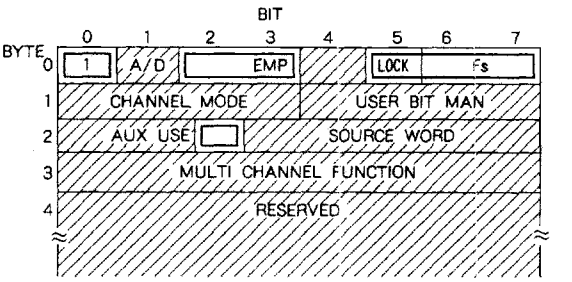
(2) Microcomputer (MODE00), Professional



(3) Easy mode (MODE01), Consumer

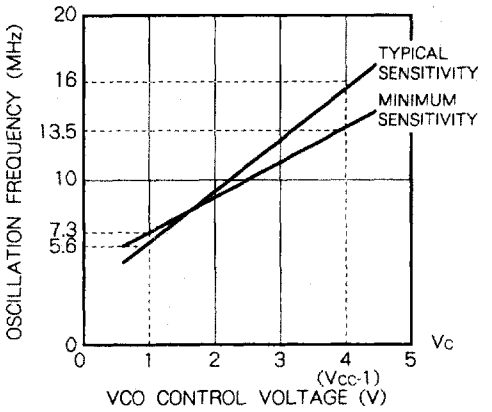


(4) Easy mode (MODE01), Professional

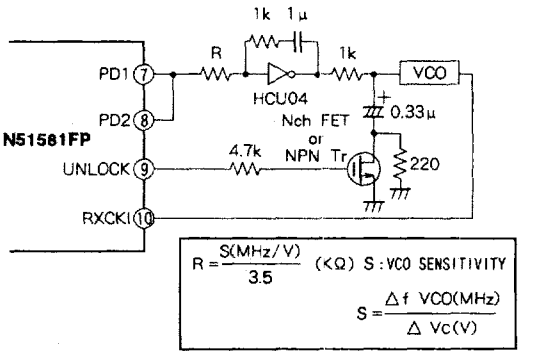


SUPPORT BIT All "0"

9. PLL APPLICATIONS



VCO Sensitivity Characteristics : Received fs = 32 to 48kHz



If VCO sensitivity is typical :

$S = \frac{16 - 5.6}{4 - 1} = 3.5(MHz/V)$ So $R = 1k\Omega$

PLL APPLICATION EXAMPLE

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10. APPLICATION EXAMPLE (MICROCOMPUTER MODE)