DATA SHEET

DIGITAL dcc COMPACT CASSETTE

SAA2003
Stereo filter and codec

Preliminary specification
File under Integrated Circuits, IC01

May 1994

Philips Semiconductors

PHILIPS

Stereo filter and codec SAA2003

FEATURES

- Single-chip stereo filter and codec
- Wide operating voltage range: 2.7 to 5.5 V
- Low-power consumption: 98 mW; 3.0 V
- Sleep mode for low power and low Electromagnetic Interference (EMI)
- Transparent serial audio data mode in sleep
- IEC 958 digital output
- Peak level detector for start of track detection or VU meter
- Versatile fade processor; slow/fast fade, mute, 12 dB attenuation
- Serial audio interface for I^2S or EIAJ formats
- Error concealment
- Three-wire L3 bus microcontroller interface
- Three sample rates:
  - 32 kHz
  - 44.1 kHz
  - 48 kHz
- Internal or external clock source
- Three programmable outputs
- Small surface mounted package (SOT307).

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

The SAA2003 performs the sub-band filtering and audio frame codec functions in the Precision Adaptive Sub-band Coding (PASC) system. It can be used as a stand-alone decoder for playback only applications, but requires the addition of an Adaptive Allocation and Scale Factor processor (SAA2013) in order to perform PASC encoding in a DCC record system.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2003H	44	QFP(1)	plastic	SOT307

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM

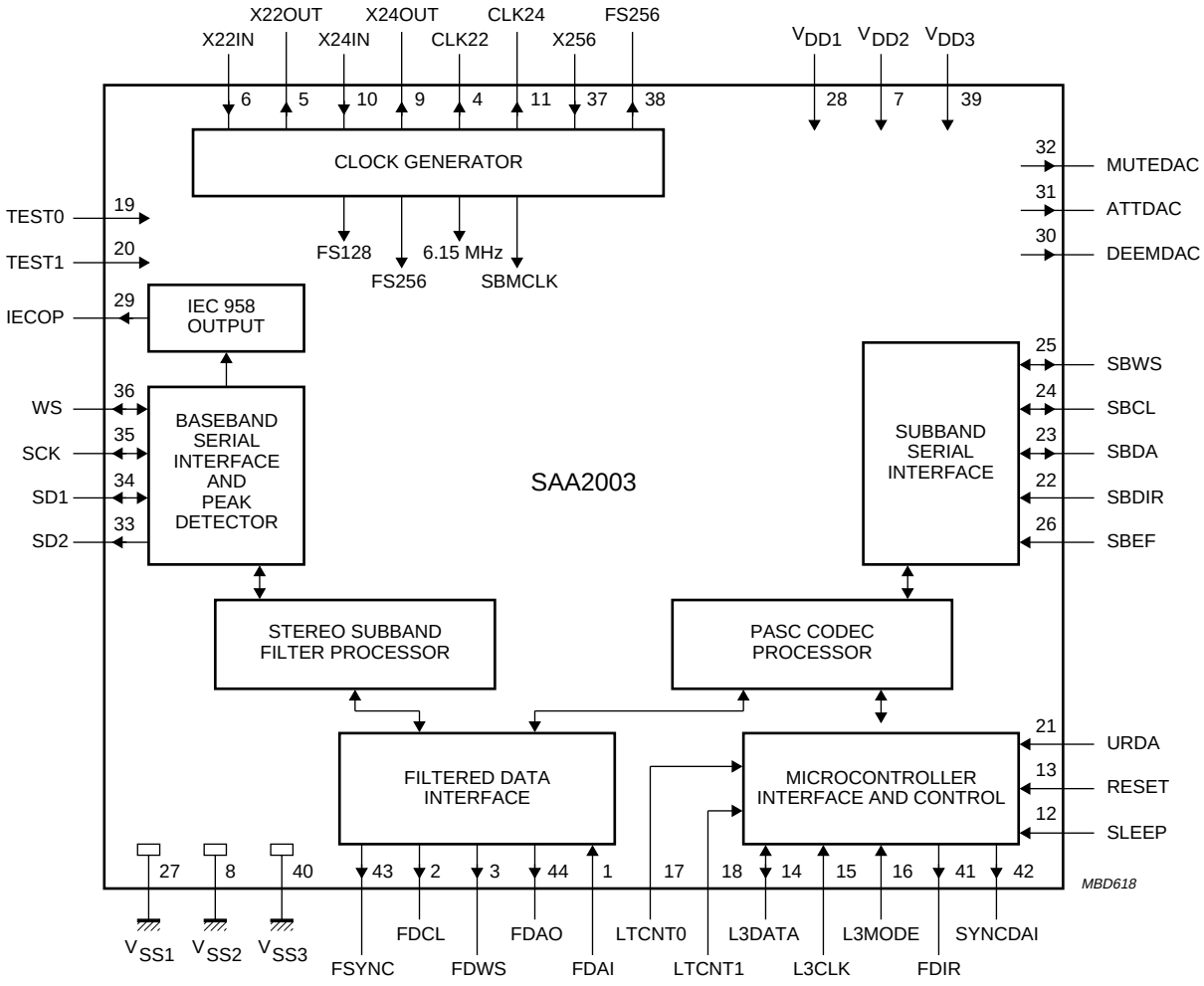


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
FDAI	1	filtered data input from SAA2013	I
FDCL	2	filtered data bit clock	O
FDWS	3	filtered data word select	O
CLK22	4	22.5792 MHz buffered clock output	O
X22OUT	5	22.5792 MHz crystal output	O
X22IN	6	22.5792 MHz crystal input	I
V_{DD2}	7	supply voltage (clock oscillator)	–
V_{SS2}	8	supply ground (clock oscillator)	–
X24OUT	9	24.576 MHz crystal output	O
X24IN	10	24.576 MHz crystal input	I
CLK24	11	24.576 MHz buffered clock output	O
SLEEP	12	sleep mode; device inactive	I
RESET	13	device reset	I
L3DATA	14	3-wire interface; serial data	I/O
L3CLK	15	3-wire interface; bit clock	I
L3MODE	16	3-wire interface; mode control	I
LTCNT0	17	LT interface; control bit 0	I
LTCNT1	18	LT interface; control bit 1	I
TEST0	19	test mode select	I
TEST1	20	test mode select	I
URDA	21	unreliable data flag from drive processor	I
SBDIR	22	sub-band data direction	I
SBDA	23	sub-band serial data	I/O
SBCL	24	sub-band bit clock	I/O
SBWS	25	sub-band word select	I/O
SBEF	26	sub-band error flag from drive processor	I
V_{SS1}	27	digital supply ground	–
V_{DD1}	28	digital supply voltage	–
IECOP	29	IEC 958 digital audio output	O
DEEMDAC	30	DAC control or general purpose output	O
ATTDAC	31	DAC control or general purpose output	O
MUTEDAC	32	DAC control or general purpose output	O
SD2	33	serial audio data to DAC	O
SD1	34	serial audio data to/from DAIO and DAC	I/O
SCK	35	serial audio data bit clock	I/O
WS	36	serial audio data word select	I/O
X256	37	master audio clock from external source	I
FS256	38	master audio clock at 256 times sample frequency	O
V_{DD3}	39	supply voltage (FS256)	–
V_{SS3}	40	supply ground (FS256)	–

SYMBOL	PIN	DESCRIPTION	TYPE
FDIR	41	filter direction; encode or decode	O
SYNCDAI	42	settings synchronization for DAIO	O
FSYNC	43	sub-band 0 sample synchronization for SAA2013	O
FDAO	44	filtered data output to SAA2013	O

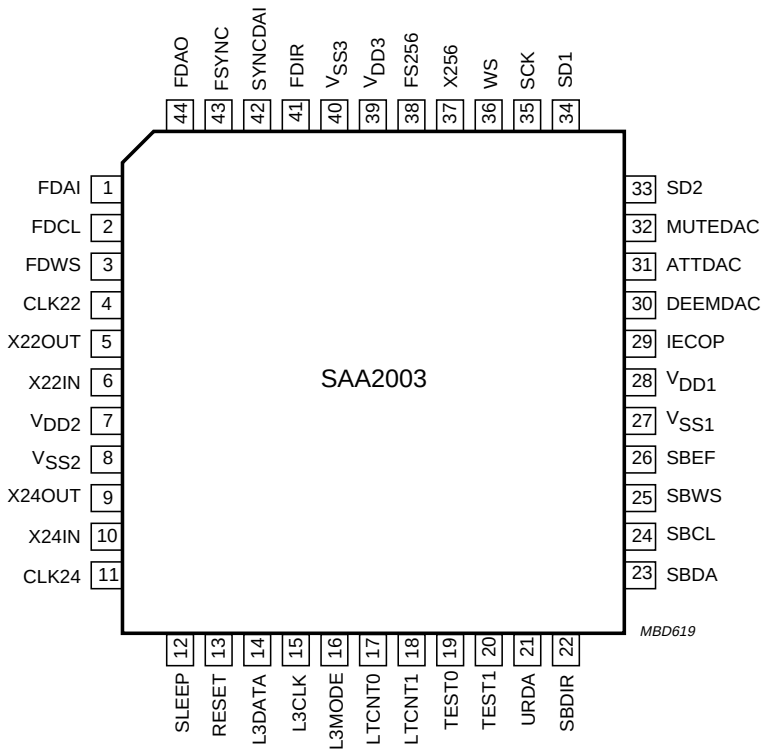


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

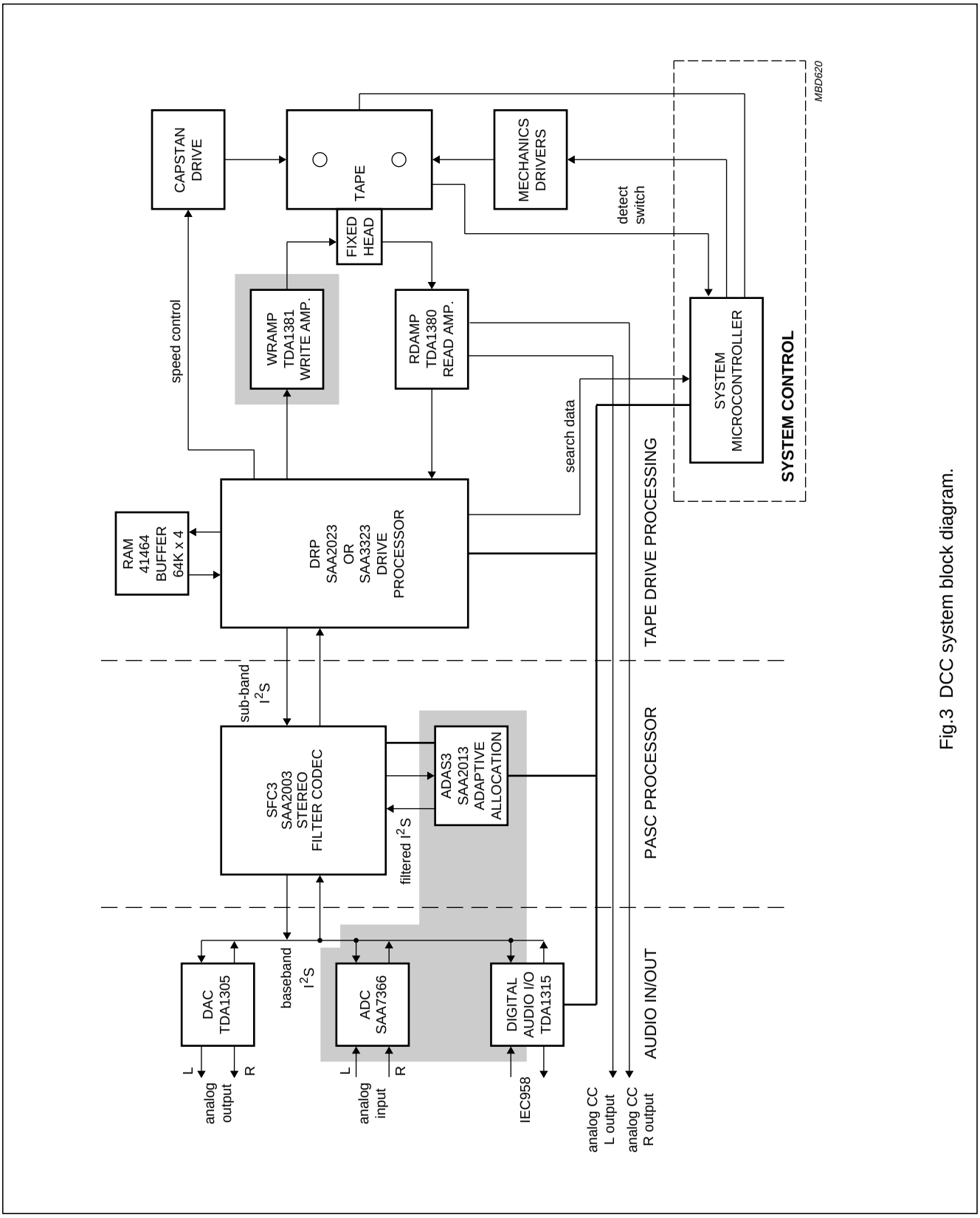


Fig.3 DCC system block diagram.

PASC processor

The PASC processor is a dedicated Digital Signal Processor (DSP) engine which efficiently codes digital audio data at a bit rate of 384 kbits/s without affecting the sound quality. This is achieved using an efficient adaptive data notation and by only encoding the information which can be heard by the human ear.

The audio data is split into 32 equal sub-bands during encoding. For each of the sub-bands a masking threshold is calculated. The samples from each of the sub-bands are included in the PASC data with an accuracy that is determined by the available bit-pool and by the difference between the signal power and the masking threshold for that sub-band.

The stereo filter codec performs the splitting (encoding) and reconstruction (decoding), including the necessary formatting functions. During encoding, the adaptive allocation and scaling circuit calculates the required accuracy (bit allocation) and scale factors of the sub-band samples.

ENCODING (SEE FIG.4)

The incoming serial audio data is filtered into 32 sub-bands for left and right (I and II) channels using the stereo filter part of the SAA2003. A PASC frame is made up of left and right (I and II) audio data for 12 samples from each of the 32 sub-bands, a total of 768 audio samples. For every PASC frame the SAA2013 calculates a bit allocation and scale factor table which is transferred to the SAA2003. All the samples in a frame are scaled in accordance with the scale factor calculated by the SAA2013. Once scaled the samples are re-quantized to reduce the number of bits to correspond with the allocation table calculated by the SAA2013. Synchronization, allocation and scale factor information is then added to provide a fully encoded PASC data signal. These frames of data are then sent to the drive processor IC (SAA2023 or SAA3323).

DECODING (SEE FIG.5)

In decoding mode the SAA2003 synchronizes and recovers frames of data from the drive processor. The recovered allocation data and the scale factors are used to correctly re-quantize and re-scale the PASC sub-band samples. The decoded sub-band samples, which are represented in 24-bits two's complement notation, are reconstructed by the sub-band filters into a single complete digital audio signal.

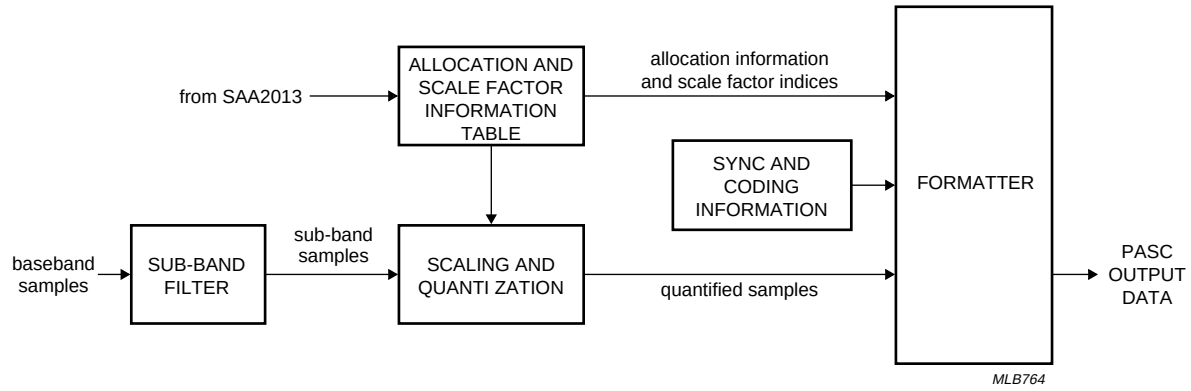


Fig.4 Encoding mode.

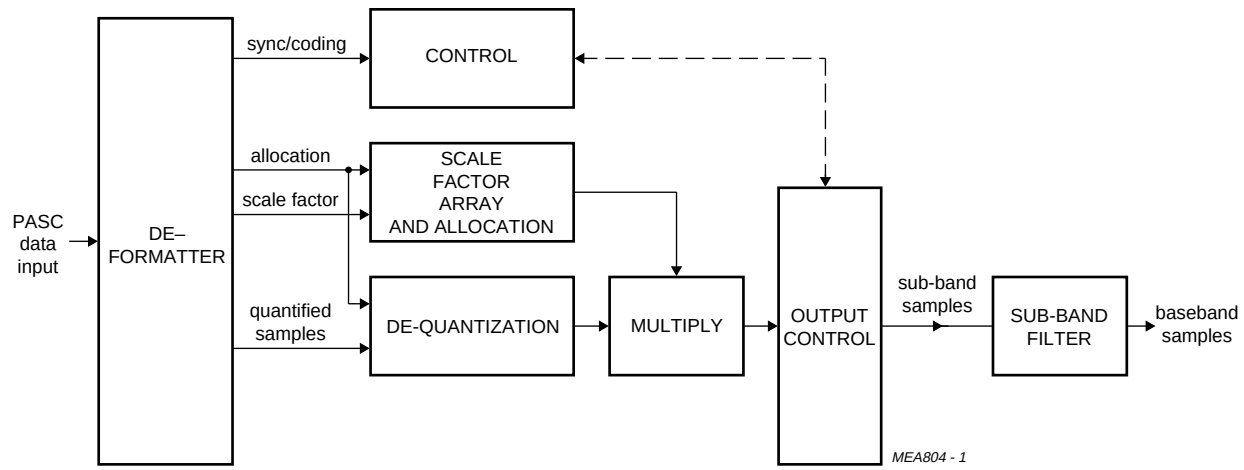


Fig.5 Decoding mode.

Crystal oscillators

The recommended crystal oscillator configuration is shown in Fig.6. The specified component values only apply to crystals with a low equivalent series resistance of <40 Ω.

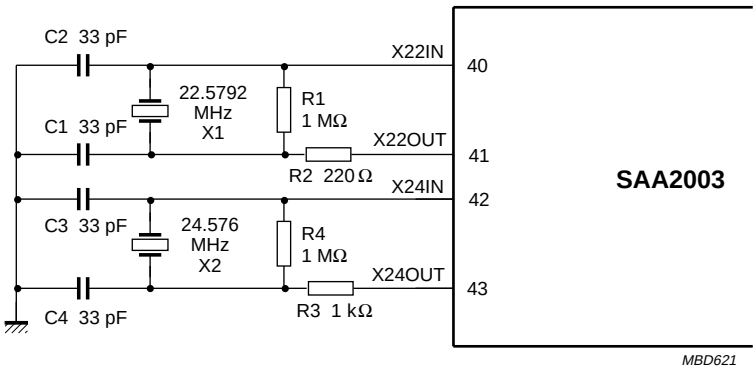


Fig.6 Crystal oscillator components.

System reset

Reset must be active from system power-up for >1 ms. Reset must also be active for >1 ms after the falling edge of sleep as shown in Fig.7.

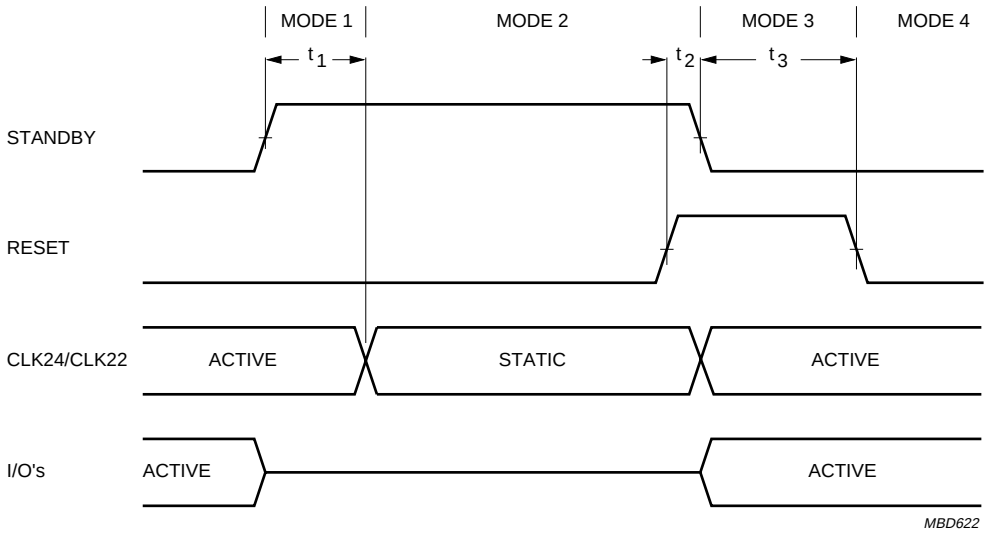


Fig.7 Reset and sleep timing.

Table 1 Reset and sleep timing modes (see Fig.7).

MODE	DESCRIPTION	TIMING	MIN.	MAX.	UNIT
MODE1	standby stage 1; clocks still running	t_1	400	–	ns
MODE2	standby mode; clocks stopped	t_2	0	–	ns
MODE3	clocks running; reset active	t_3	1	–	ms
MODE4	normal operational mode	–	–	–	

Sleep mode

A HIGH input applied to the SLEEP pin halts all internally generated clock signals. If the transparent mode of the serial audio interface is set before entering sleep, the data at the X256 external clock input is sent to the FS256 output and the data at SD1 input is sent to the SD2 output. If transparent mode is not set, these two outputs are high impedance during sleep mode.

The IECOP pin is set to high impedance during sleep mode, unless the transparent mode is selected and WS-SEL is set.

Table 2 Transparent mode function in sleep.

PIN	TRANSPARENT MODE[1]	WS-SEL[2]	PIN FUNCTION
FS256	1	X	FS256
FS256	0	X	high impedance
SD2	1	X	SD1
SD2	0	X	high impedance
IECOP	0	X	high impedance
IECOP	1	0	high impedance
IECOP	1	1	WS

Notes

1. Transparent mode is controlled by bit 3 of the serial audio data interface mode control register.
2. WS-SEL is controlled by bit 3 of the codec extended settings register.

Serial audio interface

The signals between the SAA2003 and the serial audio input/output are shown in Table 3.

Table 3 Interface signals between SAA2003 and serial audio input/output.

PIN	INPUT/OUTPUT	FUNCTION	FREQUENCY
WS	bi-directional	audio data word select	f_S
SCK	bi-directional	audio data bit clock	$64f_S$
SD1	bi-directional	serial audio data to/from DAIO and ADC	–
SD2	output	audio serial data to DAC	–
FDIR	output	PASC mode encode/decode	–
IECOP	output	alternative serial data word select for SD2	–

The word select (WS) line indicates the channel being transmitted (either left or right; I or II) and is equal in frequency to the sampling frequency (f_S).

Operating at a frequency of $64 \times f_S$, the bit clock (SCK) dictates that each WS period contains 64 SD1 or SD2 data bits. Of these bits a maximum of 36 are used to transfer data (samples may have a length up to 18 bits). Samples are transferred most significant bit (MSB) first. Both WS and SD1/SD2 change state at the negative edge of SCK.

The serial audio data is transferred between the SAA2003 and the input/output using either the standard I^2S (default) as shown in Fig.8 or the EIAJ format as shown in Fig.9.

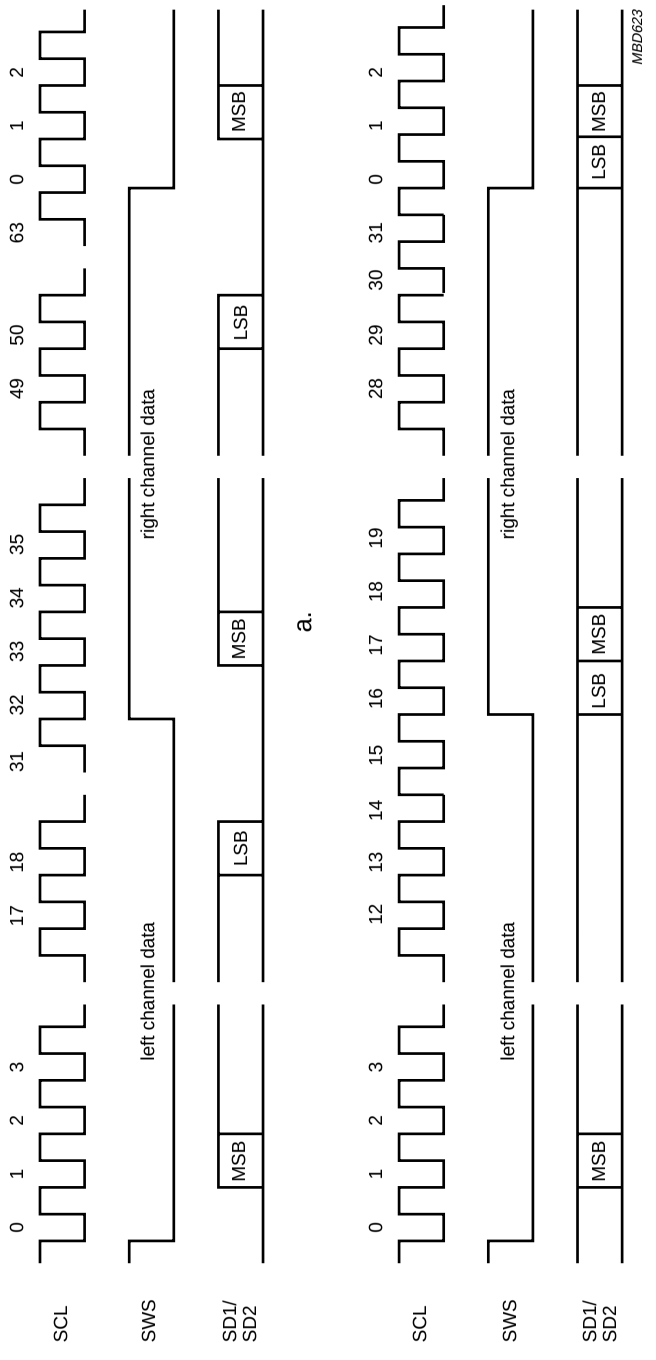


Fig.8 Serial audio interface SD1/SD2; I²S data format.

a. Master and slave modes; 18 bits.
b. Slave mode only; 16 bits.

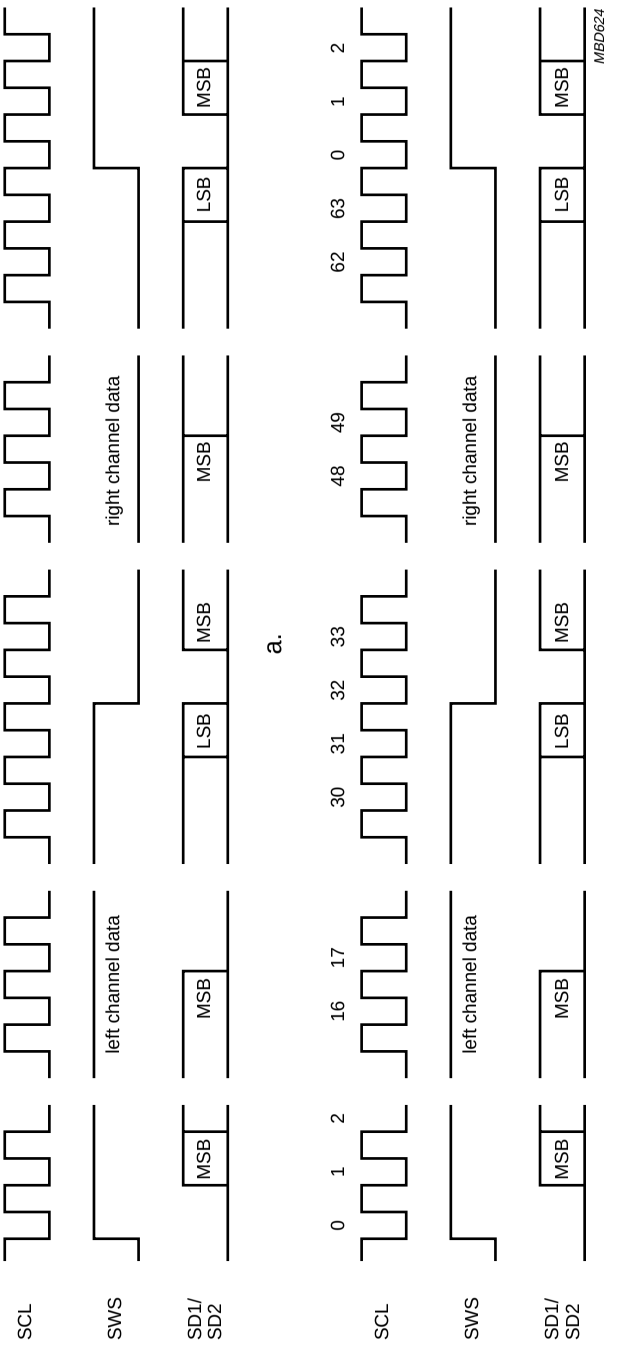


Fig.9 Serial audio interface SD1; EIAJ data format.

a. Master mode; 18 bits.
b. Master mode (EIAJ); 16 bits.

SERIAL AUDIO INTERFACE DATA FORMATS IN ENCODING MODE

In encoding mode, the serial audio data input for the PASC processor is taken from the SD1 pin. This data is scaled by the fade processor before being sent to the PASC processor. The output from the fade processor is sent in parallel to the SD2 output.

Both I^2S and EIAJ formats are supported.

Table 4 Serial audio data interface formats in encoding mode.

SD1 INPUT			SD2 OUTPUT	
FORMAT	**MASTER/SLAVE**	**RESOLUTION**	**FORMAT**	**RESOLUTION**
I^2S	master	18 bit	I^2S	18 bit
I^2S	slave	18 bit	I^2S	18 bit
I^2S	master	16 bit	I^2S	18 bit
I^2S	slave	16 bit	I^2S	16 bit
EIAJ(1)	master	18 bit	I^2S	18 bit
EIAJ(1)	slave	18 bit	I^2S	18 bit
EIAJ(1)	master	16 bit	I^2S	18 bit
EIAJ(1)	slave	16 bit	I^2S	18 bit

Note

1. If SD1 is used in EIAJ mode, and the data from SD2 is required, the IECOP can be re-programmed to provide a suitable I^2S WS signal for SD2. The IEC 958 output is not available in this mode.

SERIAL AUDIO INTERFACE DATA FORMATS IN DECODING MODE

In decoding mode, the output from the PASC processor, connected via the fade processor, is present at both SD1 and SD2.

Both I^2S and EIAJ formats are supported.

Table 5 SD1/SD2 output decoding formats.

FORMAT	MASTER/SLAVE	RESOLUTION(1)
I^2S	master	18 bit
I^2S	slave	18 bit
I^2S	master	16 bit
I^2S	slave	16 bit
EIAJ	master	18 bit
EIAJ	master	16 bit

Note

1. The sub-band filter performs rounding to 16 or 18 bits according to the operating mode of the interface.

SERIAL AUDIO INTERFACE MODE CONTROL

The operating mode of the interface is programmed by the extended settings registers as shown in Table 6.

Table 6 Extended settings register.

A3	A2	A1	A0	D3	D2	D1	D0	MODE
0	0	1	0	X	X	X	0	16 bit operation; 16 bit rounding
0	0	1	0	X	X	X	1	18 bit operation; 18 bit rounding
0	0	1	0	X	X	0	X	I^2S data format
0	0	1	0	X	X	1	X	EIAJ data format
0	0	1	0	X	0	X	X	peak detector input SD1
0	0	1	0	X	1	X	X	peak detector input SD2
0	0	1	0	0	X	X	X	SD1/FS256 transparent mode disabled
0	0	1	0	1	X	X	X	SD1/FS256 transparent mode enabled

Filtered data interface

The filtered data interface transfers the sub-band filtered data between the stereo filter codec and adaptive allocation and scaling parts of the DCC chip-set, and consists of the signals as shown in Table 7.

Table 7 Filtered data interface signals.

PIN	INPUT/OUTPUT	FUNCTION	FREQUENCY
FDCL	output	filtered data bit clock	$64f_s$
FDWS	output	filtered data word select	f_s
FDAO	output	filtered data serial output	–
FDAI	input	filtered data serial input	–
FDIR	output	decode/encode control	–
FSYNC	output	filtered data sync signal; band zero	–

FILTERED DATA INTERFACE FORMAT

The filtered data is transferred over the interface in accordance with the formats illustrated in Figs 10 and 11.

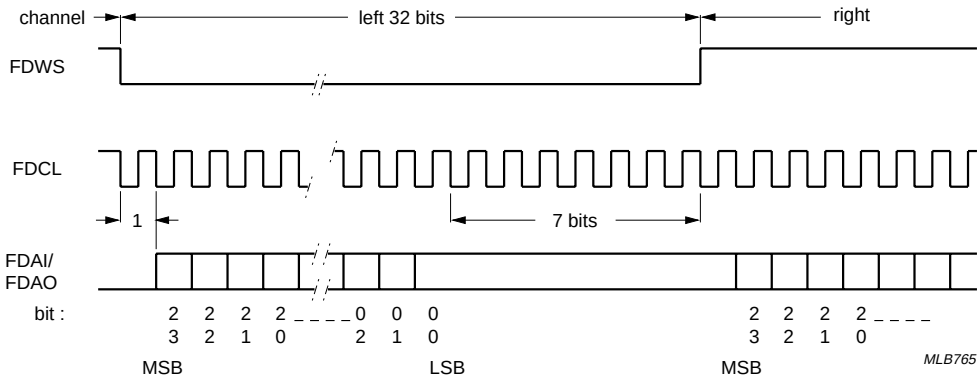


Fig.10 Transfer of filtered data; SAA2003/SAA2013.

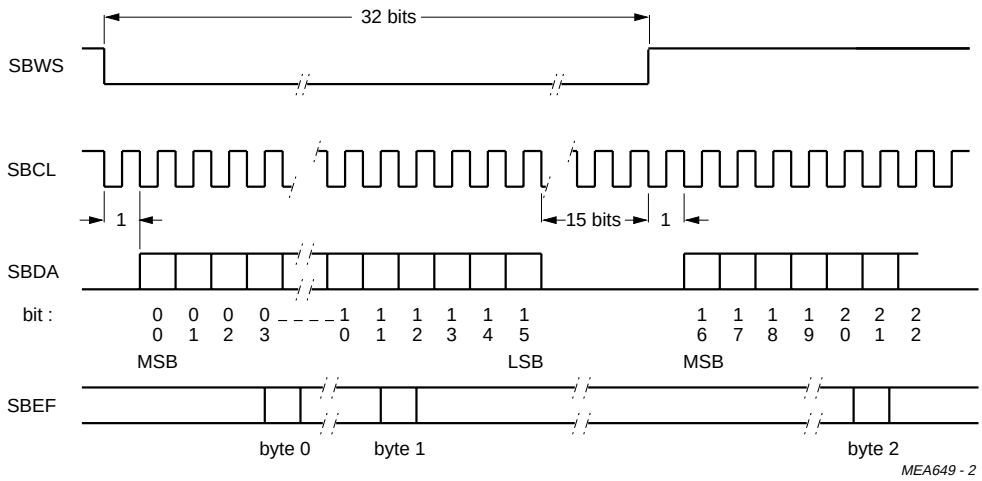


Fig.11 Transfer of sub-band PASC data.

Sub-band serial PASC interface

The sub-band serial interface carries the PASC serial data stream between the stereo filter codec and the drive processor part of the DCC chip-set, and consists of the signals as shown in Table 8.

Table 8 Sub-band serial PASC interface signals.

PIN	INPUT/OUTPUT	FUNCTION	FREQUENCY
SBDIR	input	sub-band data direction control	–
SBDA	input/output	sub-band serial data	–
1SBCL	input/output	sub-band bit clock	768 kHz
SBWS	input/output	sub-band word select	12 kHz
SBEF	input	sub-band data error flag	–
URDA	input	unreliable data flag	–

The SAA2003 generates SBWS and SBCL in both decode and encoding modes. In decode both signals can be set to inputs (slave mode) by bit 0 of the extended settings register. The filtered data interface timing is always derived from the 24.576 MHz clock, regardless of the audio sampling frequency.

Table 9 Extended settings register.

A3	A2	A1	A0	D3	D2	D1	D0	MODE
0	0	0	1	X	X	X	0	slave mode (default)
0	0	0	1	X	X	X	1	master mode

Stereo and 2-channel mono encoding modes are available. Stereo, joint stereo and 2-channel mono decoding modes are available. In decoding and encoding, 48 kHz, 44.1 kHz and 32 kHz sample frequencies can be used.

SUB-BAND SERIAL PASC INTERFACE DATA FORMAT

The PASC data is transferred over the interface described above using the format shown in Fig.11. Each period of SBWS spans 64 periods of the bit clock, SBCL, of which 32 SBCL periods are used to transfer PASC data.

The 32 data bits transferred in one period of SBWS make up a complete sub-band slot, as defined in the DCC standard. The first 16 data bits (0, 1, 2, .., 15) are transferred while SBWS is LOW, and the second 16 data bits (16, 17, 18, .., 31) are transferred while SBWS is HIGH.

SBEF and URDA are generated by the drive processor during decode. The presence of the URDA flag causes the stereo filter codec to mute the audio output data, and lose audio frame synchronization.

The direction of SBDA is controlled by the SBDIR input, which is connected to the drive processor.

SYNCDAI signal

SYNCDAI is a pulse of fixed duration which is generated by the SAA2003 when any of the following conditions occur:

- Change of bit rate
- Change of sampling frequency
- Change from encode to decode and vice-versa
- Change of FS256 clock source
- Change of I^2S bus master
- Reset.

The SYNCDAI signal is used to synchronize the digital audio input/output interface.

Audio peak level detector

The peak level detector continuously encodes the maximum amplitude of the audio data samples for each audio channel until it is reset by the action of reading out the peak level data. The peak level data can be read by the SAA2013, and subsequently by the system microcontroller, or by the microcontroller directly when SAA2013 is not used.

The peak level data is read via the L3 interface in status read mode. The first 16 bits of status read transfer the status bits of SAA2003. The following 32 bits contain the peak level data. The peak level detector is reset when the 32 bits of peak level data are read.

In encode, the peak level detector can be used to monitor the data on either SD1 (pre-fade processor) or SD2 (post fade processor). In slave EIAJ input modes the peak detection is only possible on output SD2. In decode mode, SD1 must be selected for peak detector input data.

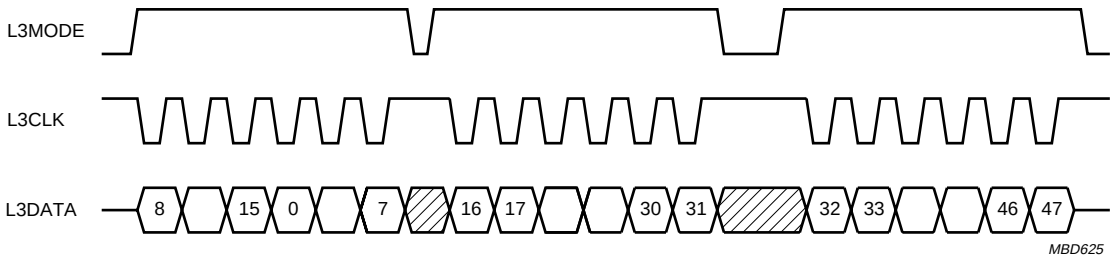


Fig.12 Peak level data format during status read.

Audio fade processor

The fade processor is controlled by the system microcontroller. It achieves level control, or fading, by multiplying the audio samples with a 17 bit accuracy fade coefficient, which is selected by an 8-bit fade counter. The fade coefficients range from 0 to 1.0 according to a $\frac{1}{4}$ cosine function. The attenuation for a particular fade count (FC) is given as follows:

$$\text{Attenuation (dB)} = -20 \log \cos\left(\frac{\pi \times FC}{510}\right)(\text{dB}) \quad \text{where: } 0 \leq FC \leq 255.$$

In encode mode, audio samples are taken from input SD1 and scaled before sub-band filter processing, and sent to output SD2.

In decode mode, audio samples are scaled following reconstruction by the sub-band filter, and sent to outputs SD1 and SD2.

Table 10 Fade processor operating modes.

MODE	FUNCTION
Fade rate	controls rate of automatic increments and decrements
Step down	increases attenuation by one increment
Step up	reduces attenuation by one increment
Full scale	sets gain to unity, incrementing from current level automatically
Mute	sets gain to zero, decrementing from current level automatically
−12 dB	sets gain to −12 dB, decrementing or incrementing from current level automatically

FADE PROCESSOR MODE CONTROL

The operating mode of the fade processor is controlled by two extended registers

Table 11 Fade processor mode control.

A3	A2	A1	A0	D3	D2	D1	D0	MODE
0	0	1	1	P3	P2	P1	P0	set fade rate
0	1	0	0	0	0	0	1	step down
0	1	0	0	0	0	1	0	step up
0	1	0	0	0	1	X	0	full scale slow
0	1	0	0	0	1	X	1	full scale fast
0	1	0	0	1	0	X	0	mute slow
0	1	0	0	1	0	X	1	mute fast
0	1	0	0	1	1	X	0	−12 dB slow
0	1	0	0	1	1	X	1	−12 dB fast
0	1	0	0	0	0	0	0	no action

FADE RATE OPTION

The fade rate can be set to either fast or slow modes. In fast mode the attenuation changes rate at one step per audio sample. In slow mode the rate of change of level is controlled by the fade rate bits P3 to P0. In slow mode, the fade counter is stepped up or down according to a clock derived from the WS pin.

Table 12 Fade rate in slow and fast modes.

MODE	P3	P2	P1	P0	TIME PER STEP (ms)			TIME FOR 256 STEPS (ms)		
					32 kHz	44.1 kHz	48 kHz	32 kHz	44.1 kHz	48 kHz
Fast	–	–	–	–	31.2 μs	22.7 μs	20.8 μs	8.0	5.8	5.3
Slow	0	0	0	0	1.0	0.997	1.0	256	255	256
Slow	0	0	0	1	2.0	1.994	2.0	512	511	512
Slow	0	0	1	1	4.0	3.988	4.0	1024	1021	1024
Slow	0	1	1	1	8.0	7.980	8.0	2048	2043	2048
Slow	1	1	1	1	16.0	15.96	16.0	4096	4087	4096

IEC 958 output

The IECOP pin provides an output signal in accordance with the IEC 958/SPDIF digital audio interface format.

The function of the IECOP pin is programmed by bit 3 of the codec extended settings register; see Table 13.

Table 13 IECOP pin control.

A3	A2	A1	A0	D3	D2	D1	D0	IECOP FUNCTION
0	0	0	1	0	X	X	X	IEC 958 (default)
0	0	0	1	1	X	X	X	I^2S word select for SD2

The IECOP output will only function when the SAA2003 is in decode mode. The IECOP cannot be used when SAA2013 is present in the system, unless the SAA2013 is in sleep mode. The IECOP output is disabled and set to high impedance by a reset.

L3 bus

The L3 bus is a three-wire clock synchronous data bus common to all ICs in the DCC chip-set. It consists of the L3MODE, L3CLK and L3DATA connections. The bus has two operating modes:

- Addressing mode; selects the IC for communication and sets type of transfer.
- Data mode; is used to send and receive data and control settings.

The L3MODE and L3CLK lines are driven by the system microcontroller and L3DATA is a bi-directional line. LTCNT0 and LTCNT1 must be left unconnected when L3 mode is used.

For normal use in L3 mode, LTCNT0 and LTCNT1 are held HIGH by internal pull-up resistors. The SAA2003 responds to serial addresses as shown in Table 14.

Table 14 SAA2003 serial addresses.

D0[1]	D1[1]	D2	D3	D4	D5	D6	D7
X	X	0	0	0	1	0	0

Note

1. D0 and D1 are interpreted as LTCNT0 and LTCNT1 respectively. These two signals control the operation of the interface as given in Table 15.

Table 15 Interface modes.

D0/LTCNT0	D1/LTCNT1	MODE
0	0	extended setting from microcontroller to SAA2003
1	0	allocation and scale factor information from SAA2013 to SAA2003
0	1	codec internal settings from microcontroller to SAA2003
1	1	codec status from SAA2003 to microcontroller and SAA2013 including peak level data

Table 16 Register address settings.

A3	A2	A1	A0	REGISTER(1)
0	0	0	0	codec external settings
0	0	0	1	codec interface mode control
0	0	1	0	serial audio interface mode control
0	0	1	1	fade counter rate control
0	1	0	0	fade counter control

Note

1. These registers are write only, accessed using the protocol shown in Fig.13.

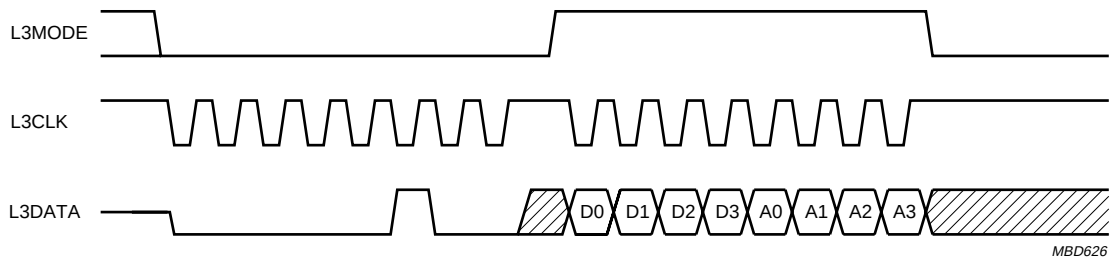


Fig.13 Extended settings protocol.

Operation in LT mode

LT interface mode can be selected by writing an extended settings word to the interface mode control register as shown in Table 17.

Table 17 Interface mode control register.

A3	A2	A1	A0	D3	D2	D1	D0	MODE
0	0	0	1	X	X	1	X	L3 mode (default)
0	0	0	1	X	X	0	X	LT mode

In LT mode the LTCNT0 and LTCNT1 pins are used, and the L3MODE pin becomes LTEN enable line. L3CLK becomes LTCLK, and L3DATA becomes LTDATA.

Table 18 Summary of address registers.

ADDRESS REGISTER		BIT	DESCRIPTION
REGISTER	**EXPLANATION**		
0	external settings register	0	mute DAC
		1	attenuate DAC
		2	de-emphasis DAC
		3	clock OK hold mode
1	codec extended settings	0	slave receive mode
		1	L3/LT mode select
		2	comparator delay bypass
		3	WS/IEC 958 selection
2	serial audio mode control	0	18 bit operation
		1	I^2S/EIAJ format
		2	peak detector input select
		3	transparent mode
3	fade processor fade rate	0 to 3	rate control, 0 to 15
4	fade processor control	0 to 3	fade command
5 to 15	not used	–	–

Codec internal settings and status

The settings register is write only, and the status register is read only. The interface protocols for accessing these registers is shown in Figs 14 and 15.

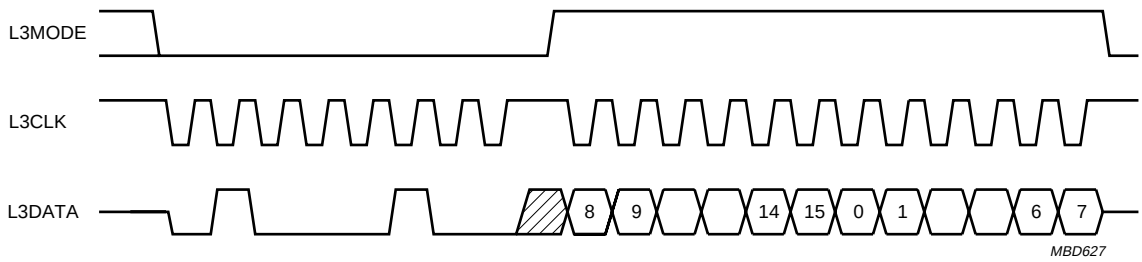


Fig.14 Codec internal settings write transfer.

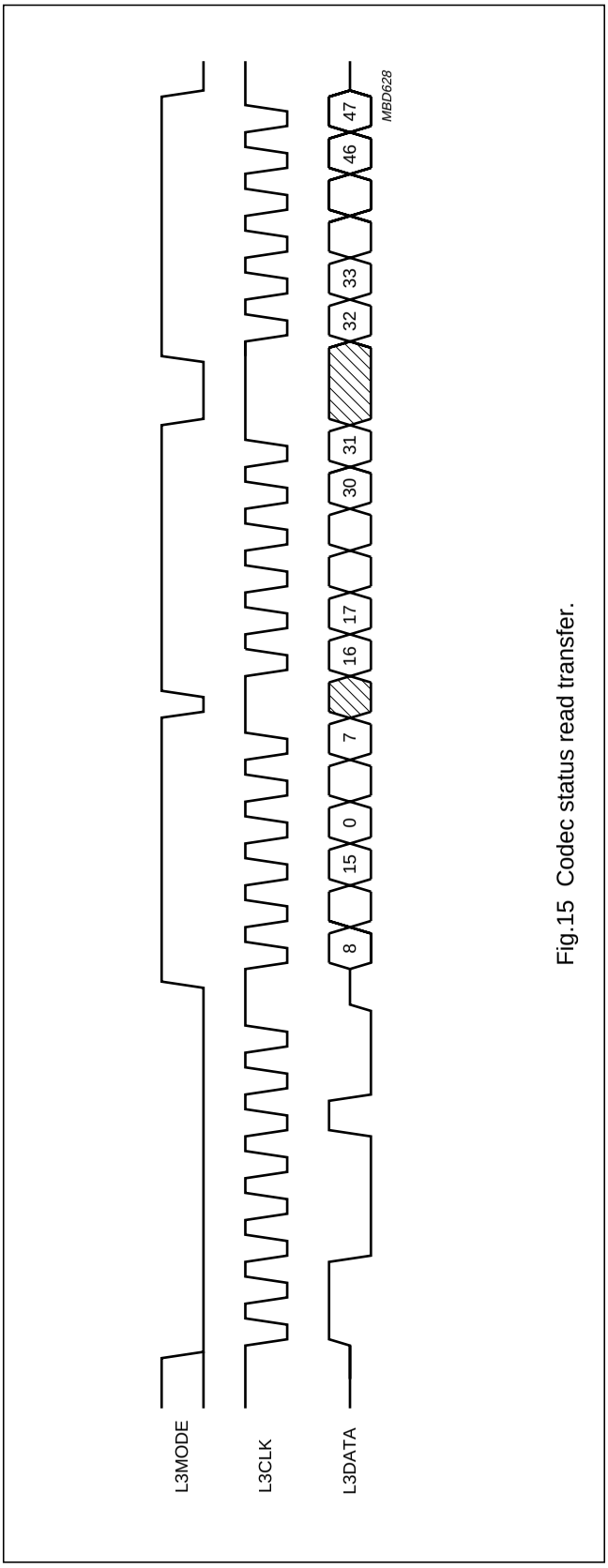


Fig.15 Codec status read transfer.

The codec internal settings register is shown in Table 19.

Table 19 Codec internal settings register formats.

BITS	DESCRIPTION	ENCODING/DECODING
15 to 12	bit rate index	encoding only
11 and 10	sample frequency	encoding only
9	decode mode	encoding and decoding
8	external FS256	encoding and decoding
7	2 channel mono	encoding only
6	mute sub-band filters	encoding and decoding
5	external master I^2S	encoding and decoding
4	select channel I/II	decoding only
3 and 2	transparent bits	encoding only
1 and 0	emphasis indication	encoding only

Table 20 Codec status register formats.

BITS	DESCRIPTION	ENCODING/DECODING
15 to 12	bit rate index	encoding and decoding
11 and 10	sample frequency	encoding and decoding
9	ready-to-receive	encoding and decoding
8	not used	–
7 and 6	sub-band mode	encoding and decoding
5	synchronization	decoding only
4	clock OK	encoding and decoding
3 and 2	transparent bits	encoding and decoding
1 and 0	emphasis indication	encoding and decoding
16	first channel identification	–
17 to 31	first channel peak level; LSB first	–
32	second channel identification	–
33 to 47	second channel peak level; LSB first	–

Average current consumption

The average current consumption is shown in Fig.16.

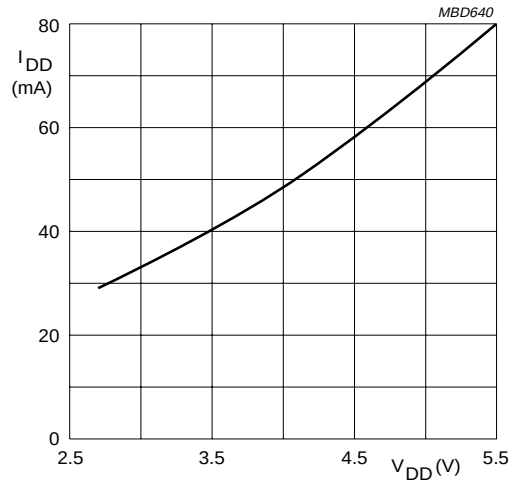


Fig.16 Average current consumption.

Timing diagrams

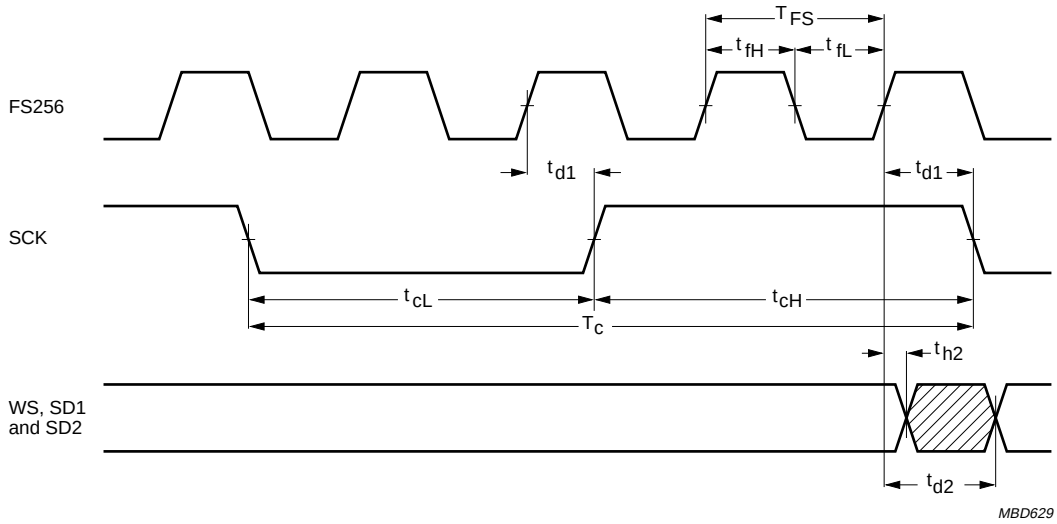


Fig.17 Serial audio interface timing in decode; master mode.

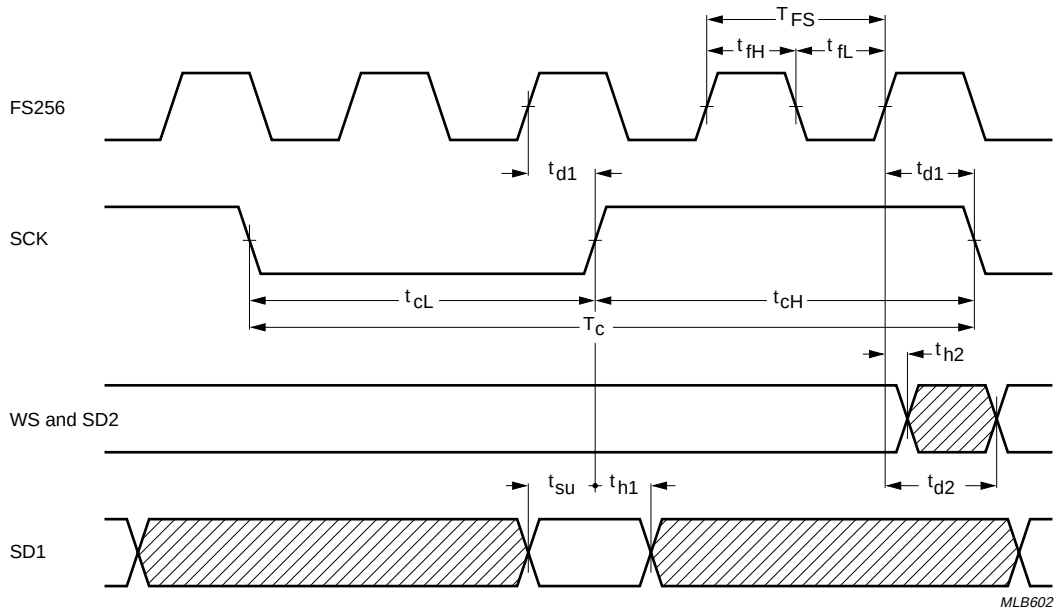


Fig.18 Serial audio interface timing in encode; master mode.

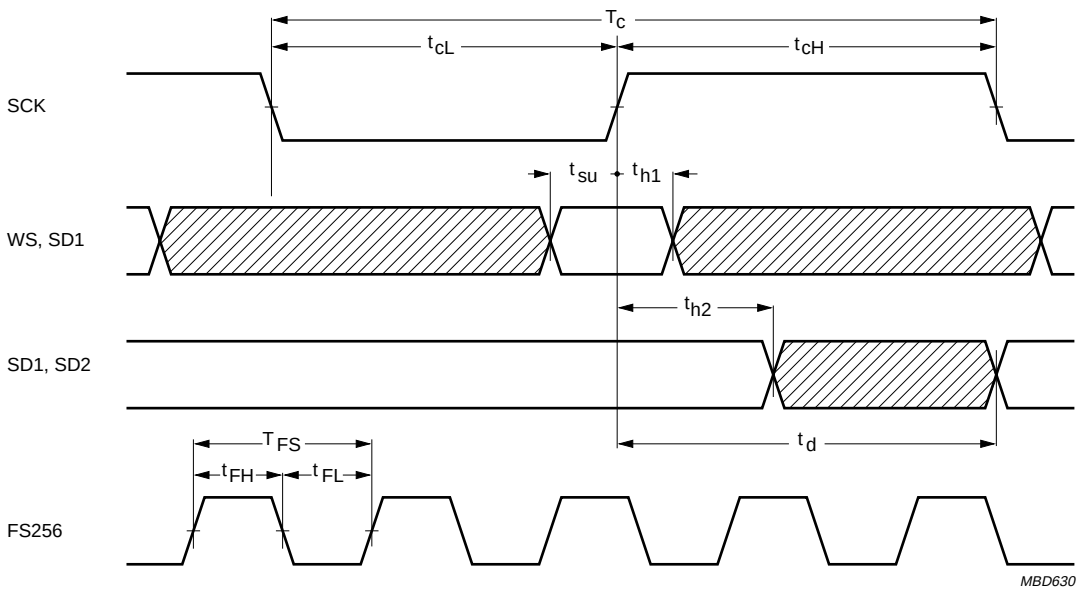


Fig.19 Serial audio interface timing; slave mode.

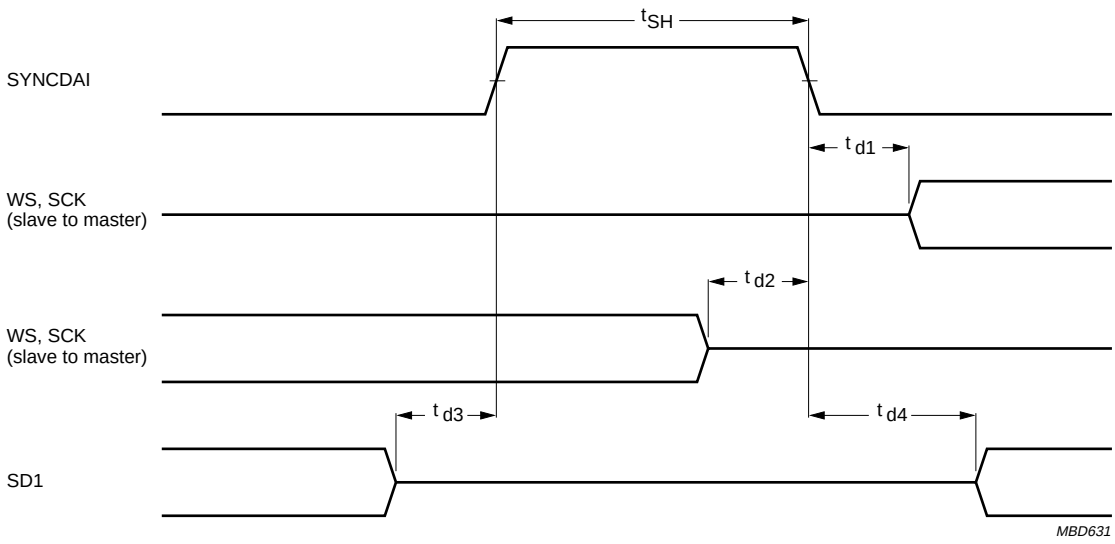


Fig.20 Serial audio master/slave timing.

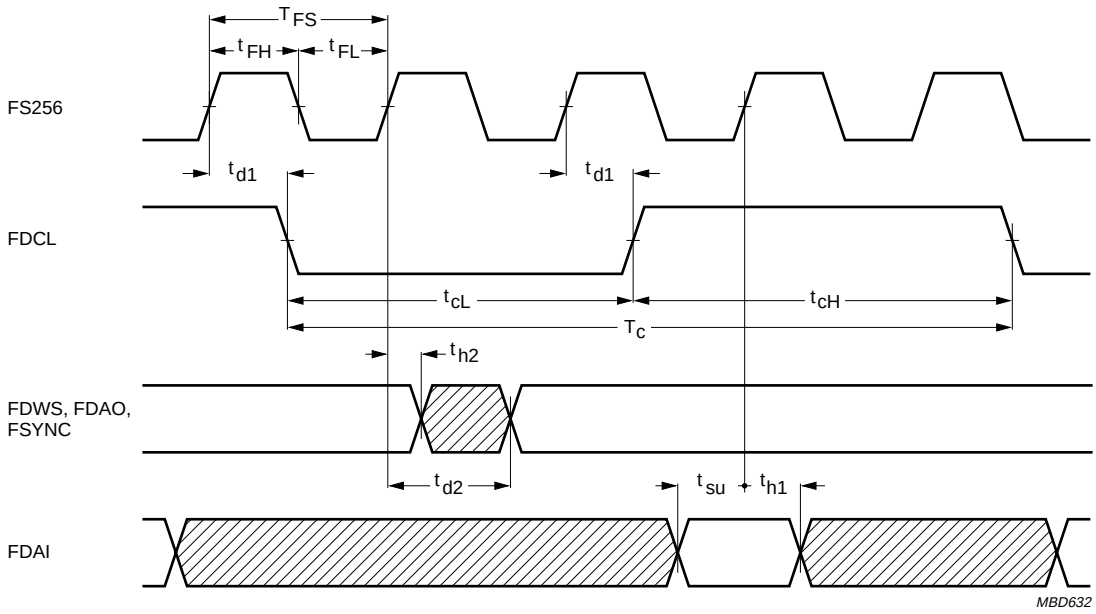


Fig.21 Filtered data interface timing.

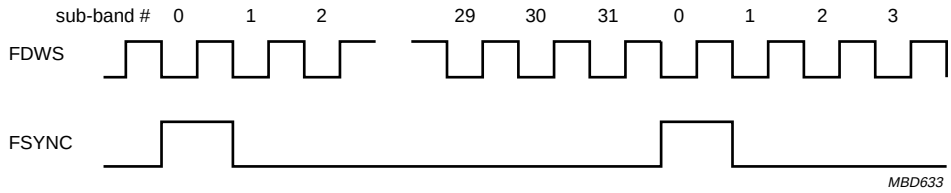


Fig.22 FSYNC output timing.

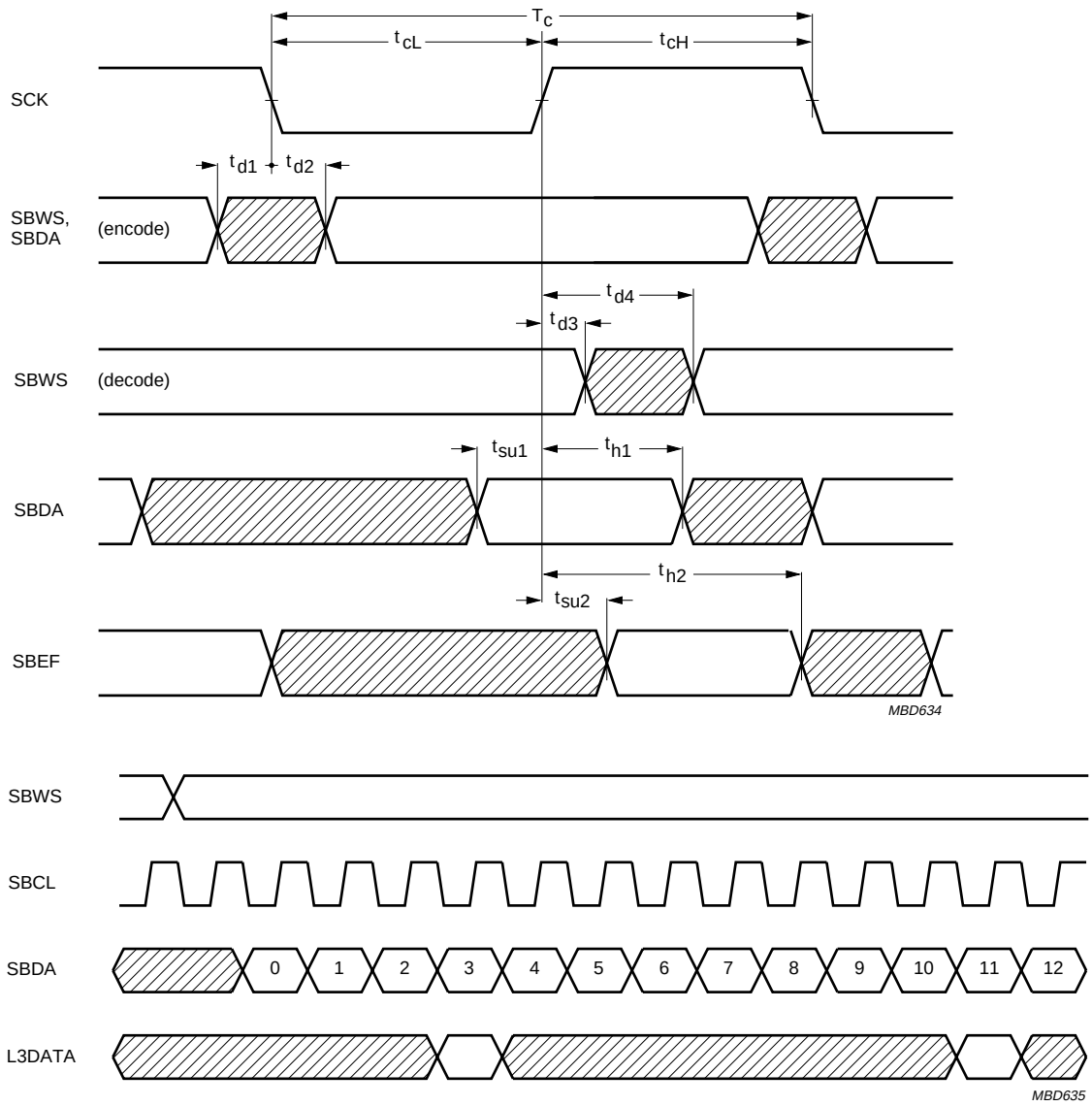


Fig.23 Sub-band PASC interface timing.

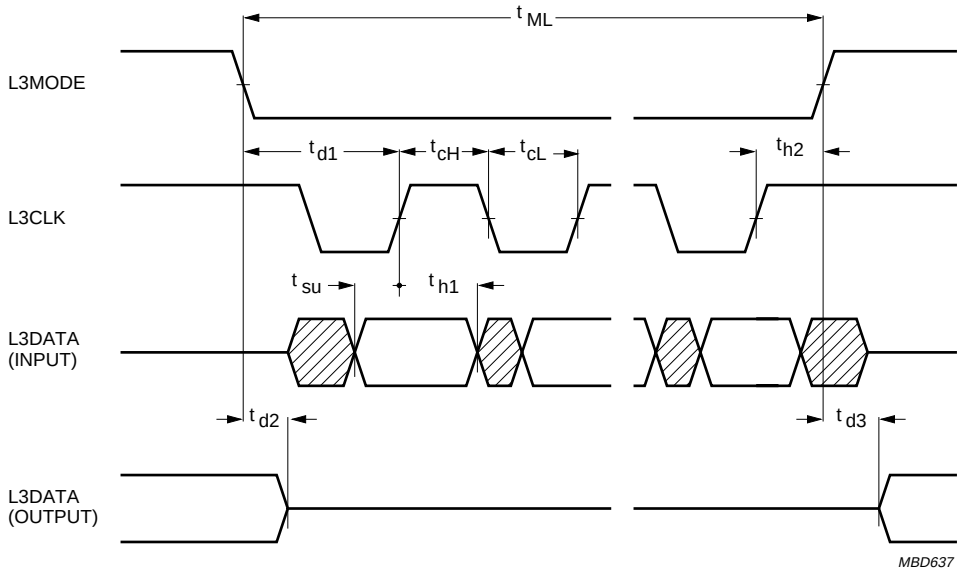


Fig.24 L3 bus timing; addressing mode.

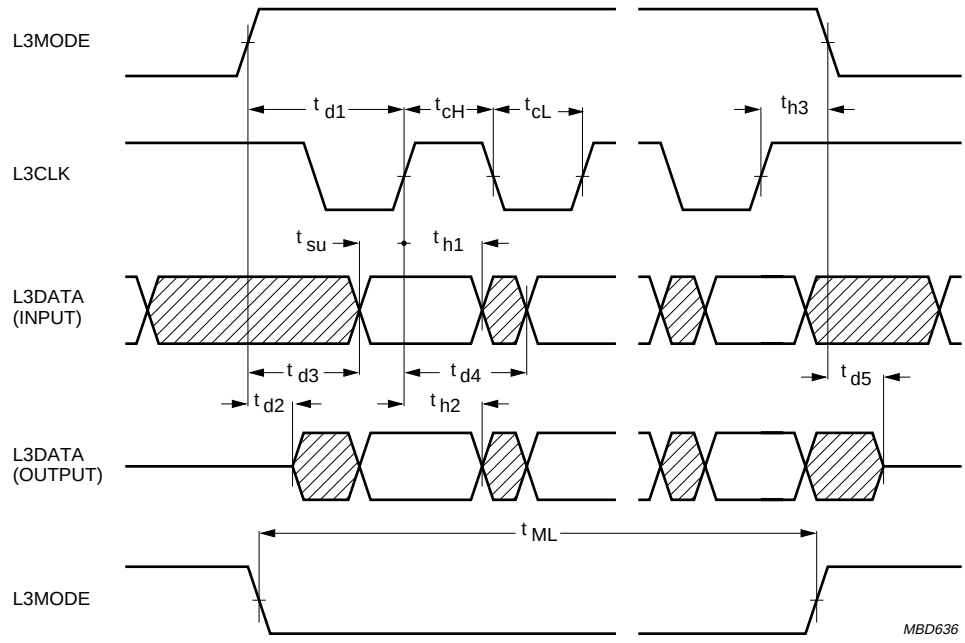


Fig.25 L3 bus timing; data transfer mode.

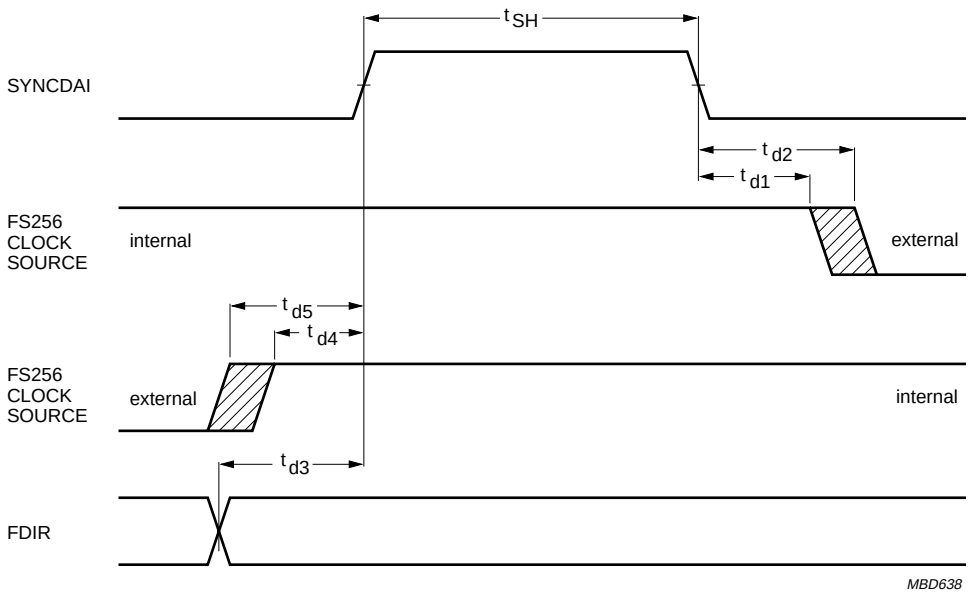


Fig.26 Internal/external clock source transition timing.

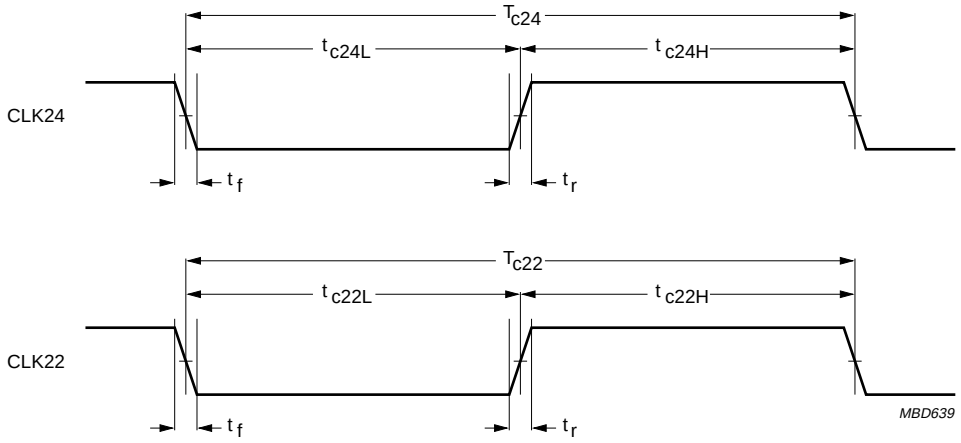


Fig.27 CLK22 and CLK24 timing.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+6.5	V
V_I	input voltage	note 1	–0.5	V_{DD} + 0.5	V
I_I	input current		–	20	mA
V_O	output voltage		–0.5	+6.5	V
I_O	output current		–	20	mA
I_{DDQ}	quiescent supply current	clocks stopped	–	100	µA
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es1}	electrostatic handling	note 2	–2000	+2000	V
V_{es2}	electrostatic handling	note 3	–200	+200	V

Notes

1. The input voltage (V_I) may not exceed 6.5 V.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
3. Equivalent to discharging a 200 pF capacitor through a 2.5 µH inductor.

CHARACTERISTICS

T_{amb} = –40 to 85 °C; V_{DD} = 2.7 to 5.5 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 3.0 V	–	32.5	35.0	mA
		V_{DD} = 5.0 V	–	68.8	75.0	mA
		sleep mode; V_{DD} = 5.0 V	–	–	400	µA
Inputs FDAI, L3CLK, URDA, SBDIR, SBEF, X256, SLEEP and L3MODE						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
Inputs TEST0 and TEST1						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
$R_{I(pd)}$	input pull-down resistance	$V_I = V_{DD}$	–	50	–	kΩ
C_I	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs LTCNT0 and LTCNT1						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
$R_{I(pu)}$	input pull-up resistance	V_I = 0 V	–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
Input RESET						
V_{tLH}	threshold voltage LOW-to-HIGH		–	–	$0.8V_{DD}$	V
V_{tHL}	threshold voltage HIGH-to-LOW		$0.2V_{DD}$	–	–	V
V_{hys}	hysteresis voltage		–	$0.33V_{DD}$	–	V
C_I	input capacitance		–	–	10	pF
Outputs FDCL, FDWS, FDIR, FSYNC, FDAO, MUTEDAC, ATTDAC and DEEMDAC						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	30	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 30 pF	–	–	20	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 30 pF	–	–	20	ns
Output CLK22						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	30	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 30 pF	–	–	7	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 30 pF	–	–	7	ns
Output CLK24						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –6 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 50 pF	–	–	7	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 50 pF	–	–	7	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output SYNCDAI						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	40	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 40 pF	–	–	20	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 40 pF	–	–	20	ns
Output FS256						
V_{OL}	LOW level output voltage	I_{OL} = 6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –6 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	60	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 60 pF	–	–	7	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 60 pF	–	–	7	ns
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
Output SD2						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	30	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 30 pF	–	–	20	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 30 pF	–	–	20	ns
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
Output IECOP						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 50 pF	–	–	20	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 50 pF	–	–	20	ns
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs/outputs SBDA, SBCL and SBWS						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
$R_{I(pd)}$	input pull-down resistance	$V_I = V_{DD}$	–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	30	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 30 pF	–	–	20	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 30 pF	–	–	20	ns
Inputs/outputs SD1, SCK and WS						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
$R_{I(pd)}$	input pull-down resistance	$V_I = V_{DD}$	–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 50 pF	–	–	20	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 50 pF	–	–	20	ns
Input/output L3DATA						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	60	pF
t_r	output rise time	0.4 V to V_{DD} – 0.4 V; C_L = 60 pF	–	–	20	ns
t_f	output fall time	V_{DD} – 0.4 V to 0.4 V; C_L = 60 pF	–	–	20	ns
Input X22IN (external clock)						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current		–10	–	+10	μA
C_I	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output X22OUT						
f_{xtal}	crystal frequency	note 1	–	22.5792	–	MHz
g_m	transconductance		1.5	–	–	mS
G_v	small signal voltage gain	$G_v = g_m \times R_O$	3.5	–	–	
C_{fb}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF
Input X24IN (external clock)						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current		–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
Output X24OUT						
f_{xtal}	crystal frequency	note 1	–	24.567	–	MHz
g_m	transconductance		1.5	–	–	mS
G_v	small signal voltage gain	$G_v = g_m \times R_O$	3.5	–	–	
C_{fb}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF
Input X256						
f_i	input frequency	f_s = 48 kHz	–	12.288	–	MHz
		f_s = 44.1 kHz	–	11.2896	–	MHz
		f_s = 32 kHz	–	8.192	–	MHz
t_{cH}	HIGH time		35	–	–	ns
t_{cL}	LOW time		35	–	–	ns
CLK22 and CLK24 timing; Fig.27						
OUTPUT CLK24						
f_o	output frequency	C_L = 50 pF	–	24.576	–	MHz
t_{c24H}	HIGH time	C_L = 50 pF	12	–	–	ns
t_{c24L}	LOW time	C_L = 50 pF	12	–	–	ns
t_r	rise time	C_L = 50 pF	–	–	7	ns
t_f	fall time	C_L = 50 pF	–	–	7	ns
OUTPUT CLK22						
f_o	output frequency	C_L = 30 pF	–	22.5792	–	MHz
t_{c22H}	HIGH time	C_L = 30 pF	11	–	–	ns
t_{c22L}	LOW time	C_L = 30 pF	11	–	–	ns
t_r	rise time	C_L = 30 pF	–	–	7	ns
t_f	fall time	C_L = 30 pF	–	–	7	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drive processing interface timing; see Fig.23						
t_{cy}	SCK cycle time		–	1302	–	ns
t_{cH}	SCK HIGH time		460	651	–	ns
t_{cL}	SCK LOW time		460	651	–	ns
t_{d1}	SBWS and SBDA delay time until SCK LOW		20	–	–	ns
t_{d2}	SCK delay time until SBWS and SBDA valid		–	–	20	ns
t_{su1}	SBDA input set-up time before SCK HIGH		235	–	–	ns
t_{h1}	SBDA input hold time after SCK HIGH		30	–	–	ns
t_{su2}	set-up time from SCK HIGH until SBEF valid		–	–	90	ns
t_{h2}	SBEF input hold time after SCK HIGH		380	–	–	ns
Filtered data interface timing; see Fig.21						
FDCL, FDWS, FDAI AND FDAO						
f_{256}	FS256 frequency	f_s = 48 kHz	–	12.288	–	MHz
		f_s = 44.1 kHz	–	11.2896	–	MHz
		f_s = 32 kHz	–	8.192	–	MHz
T_c	FDCL cycle time	f_s = 48 kHz	–	325.6	–	ns
t_{FH}	FS256 HIGH time	f_s = 48 kHz; note 2	35	–	–	ns
		f_s = 44.1 kHz; note 2	38	–	–	ns
		f_s = 32 kHz; note 2	75	–	–	ns
t_{FL}	FS256 LOW time	f_s = 48 kHz; note 2	35	–	–	ns
		f_s = 44.1 kHz; note 2	38	–	–	ns
		f_s = 32 kHz; note 2	35	–	–	ns
t_{d1}	FS256 delay time until FDCL transition		0	–	50	ns
t_{cH}	FDCL HIGH time	f_s = 48 kHz	143	–	–	ns
t_{cL}	FDCL LOW time	f_s = 48 kHz	143	–	–	ns
t_{h2}	FDWS, FDAO and FSYNC hold time after FS256 HIGH		0	–	–	ns
t_{d2}	FS256 HIGH delay time until FDWS, FDAO and FSYNC valid		0	–	50	ns
t_{su}	FDAI input set-up time before FS256 HIGH		20	–	–	ns
t_{h1}	FDAI input hold time after FS256 HIGH		30	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing characteristics FDIR and SYNCDAI; see Fig.26						
t_{sH}	SYNCDAI HIGH time		1280	–	–	ns
t_{d1}	internal clock delay time after SYNCDAI LOW		0	–	–	ns
t_{d2}	external clock delay time after SYNCDAI LOW		–	–	320	ns
t_{d3}	FDIR delay time before SYNCDAI HIGH		280	–	–	ns
t_{d4}	external clock delay time before SYNCDAI HIGH		–	–	320	ns
t_{d5}	internal clock delay time before SYNCDAI HIGH		0	–	–	ns
Baseband data interface timing characteristics						
MASTER MODE; SEE FIGS 17 AND 18						
T_c	SCK cycle time	f_s = 48 kHz	–	325.6	–	ns
t_{cH}	SCK HIGH time	f_s = 48 kHz	143	–	–	ns
t_{cL}	SCK LOW time	f_s = 48 kHz	143	–	–	ns
t_{d1}	FS256 HIGH delay time until SCK transition		0	–	50	ns
t_{h2}	WS, SD1 and SD2 hold time after FS256 HIGH		0	–	–	ns
t_{d2}	FS256 delay time until WS, SD1 and SD2 valid		0	–	50	ns
t_{su}	SD1 input set-up time before SCK HIGH		30	–	–	ns
t_{h1}	SD1 input hold time after SCK HIGH		0	–	–	ns
SLAVE MODE; SEE FIG.19						
T_c	SCK cycle time	f_s = 48 kHz	325.6	–	651.2	ns
t_{cH}	SCK HIGH time	f_s = 48 kHz	116	–	–	ns
t_{cL}	SCK LOW time	f_s = 48 kHz	116	–	–	ns
t_{su}	WS and SD1 inputs set-up time before SCK HIGH		30	–	–	ns
t_{h1}	WS and SD1 inputs hold time after SCK HIGH		0	–	–	ns
t_{h2}	SD1 and SD2 outputs hold time after SCK HIGH		66	–	–	ns
t_d	SCK delay time until SD1 and SD2 outputs valid		–	–	223	ns

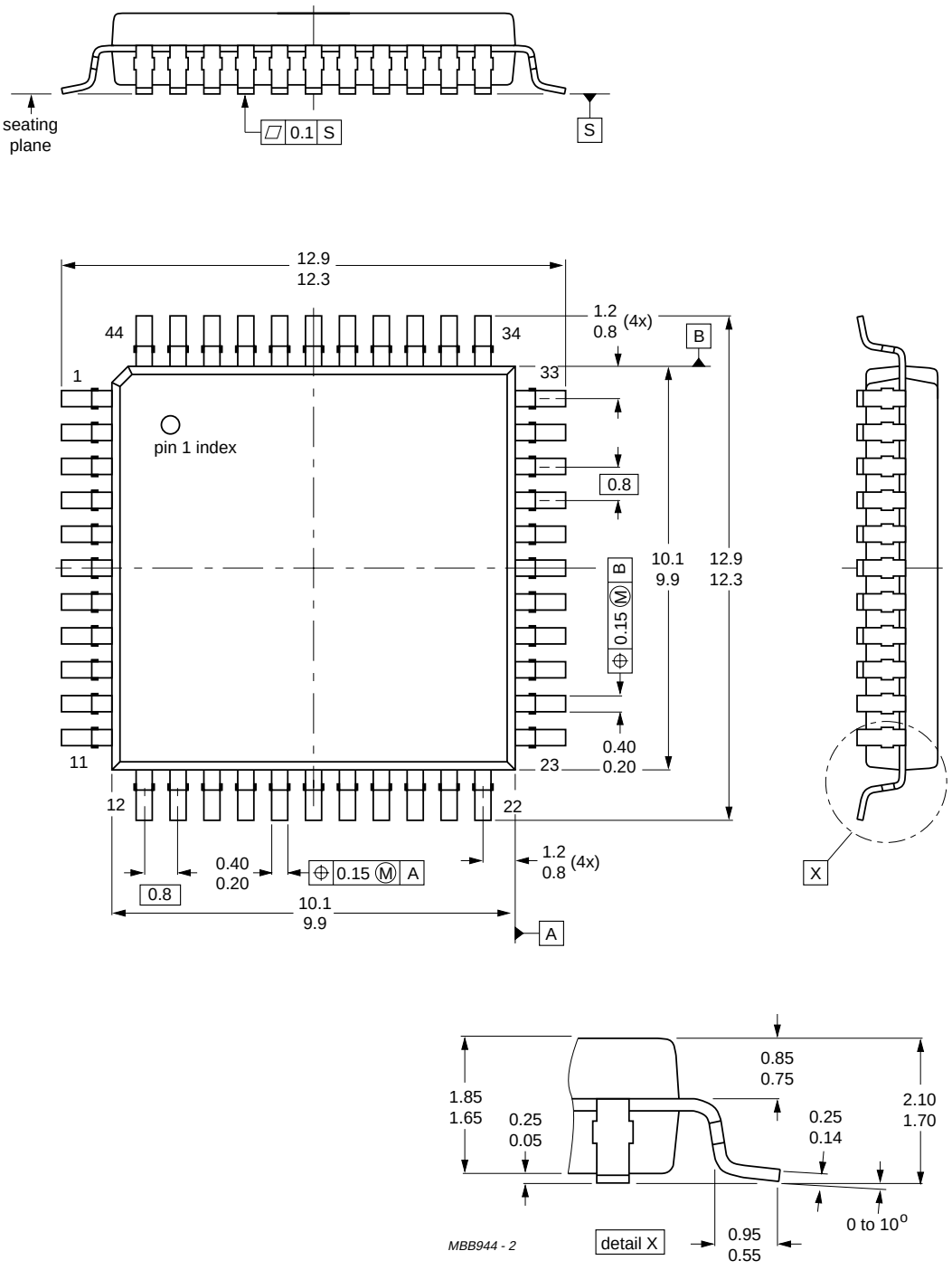
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing characteristics master/slave mode transition; see Fig.20						
t_{sH}	SYNCDAI HIGH time		1280	–	–	ns
t_{d1}	WS and SCK outputs enabled after SYNCDAI LOW		140	–	–	ns
t_{d2}	WS and SCK outputs disabled before SYNCDAI LOW		140	–	–	ns
t_{d3}	SD1 output disabled before SYNCDAI HIGH		250	–	–	ns
t_{d4}	SD1 output enabled after SYNCDAI LOW		790	–	–	ns
Timing L3 interface; see Fig.24						
ADDRESSING MODE						
t_{cH}	L3CLK HIGH time		210	–	–	ns
t_{cL}	L3CLK LOW time		210	–	–	ns
t_{d1}	L3MODE LOW delay time until L3CLK HIGH		190	–	–	ns
t_{su}	L3DATA input set-up time before L3CLK HIGH		190	–	–	ns
t_{h1}	L3DATA input hold time after L3CLK HIGH		30	–	–	ns
t_{h2}	L3CLK HIGH hold time before L3MODE HIGH		190	–	–	ns
t_{d2}	L3MODE LOW delay time until L3DATA disabled		0	–	50	ns
t_{d3}	L3MODE HIGH delay time until L3DATA enabled		0	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DATA MODE; SEE FIG.25						
t_{cH}	L3CLK HIGH time		210	–	–	ns
t_{cL}	L3CLK LOW time		210	–	–	ns
t_{d1}	L3MODE delay time until L3CLK HIGH		190	–	–	ns
t_{d2}	L3MODE delay time until L3DATA enabled		0	–	50	ns
t_{d3}	L3MODE delay time until L3DATA valid		–	–	380	ns
t_{su}	L3DATA set-up time before L3CLK HIGH		190	–	–	ns
t_{h1}	L3DATA input hold time after L3CLK HIGH		30	–	–	ns
t_{h2}	L3DATA output hold time after L3CLK HIGH		120	–	–	ns
t_{d4}	L3CLK delay time until L3DATA output valid	not between data bits 7 and 8	–	–	360	ns
		between data bits 7 and 8	–	–	530	ns
t_{h3}	L3CLK HIGH hold time before L3MODE LOW		190	–	–	ns
t_{d5}	L3MODE LOW delay time until L3DATA output disabled		0	–	50	ns
t_{ML}	L3MODE LOW time	between data words	190	–	–	ns

Notes

1. The crystal frequencies 22.5792 MHz $\pm 200 \times 10^{-6}$ MHz and 24.5760 MHz $\pm 200 \times 10^{-6}$ MHz must track each other in frequency with an accuracy of 200×10^{-6} MHz. For example if the 24.5760 MHz clock is 150×10^{-6} MHz fast, then the range of the 22.5792 MHz clock becomes -50×10^{-6} MHz and $+350 \times 10^{-6}$ MHz
2. Timing values only valid for internally generated FS256.

PACKAGE OUTLINE



Dimensions in mm.

Fig.28 Plastic quad flat-pack, 44-pin (short) (QFP44SL).

SOLDERING

Plastic quad flat-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands

513061/1500/01/pp44 Date of release: May 1994

Document order number: 9397 731 40011

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