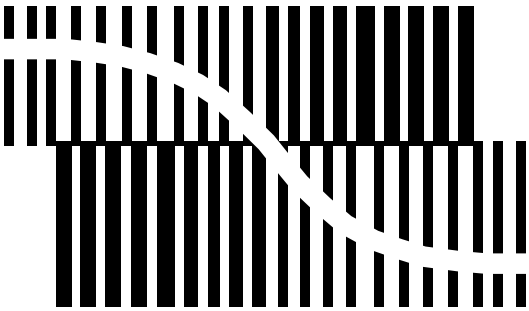
DATA SHEET



BITSTREAM CONVERSION

SAA7366
Bitstream conversion ADC for digital audio systems

Preliminary specification
File under Integrated Circuits, IC01

May 1994

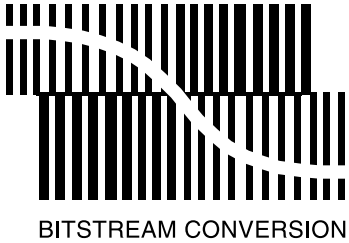
PHILIPS

Bitstream conversion ADC for digital audio systems

SAA7366

FEATURES

- Integrated buffers for simple interfacing to analog inputs
- 4 flexible serial interface modes
- Overload detection of digital signal ≥–1 dB amplitude
- Selectable high-pass filter
- 18-bit serial output
- 3.4 to 5.5 V operation of digital part
- Standby mode
- SO24 package
- Small non-critical PCB layout.



GENERAL DESCRIPTION

The SAA7366 is a CMOS cost effective stereo analog-to-digital converter (ADC) using the Philips bitstream conversion technique.

APPLICATIONS

The device is designed for digital acquisition of analog audio signals for digital audio systems such as:

- CD-recordable
- Digital Compact Cassette (DCC)
- Digital Audio Tape (DAT).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	3.4	5.0	5.5	V
V_{DDA}	analog supply voltage	4.5	5.0	5.5	V
f_i	clock input frequency	4.608	12.288	13.568	MHz
THD + N	total harmonic distortion + noise	–	–	–80	dB
DR	dynamic range	90	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7366T(1)	24	SO24L	plastic	SOT137A

Note

1. Plastic small outline package; 24 leads; body width 7.5 mm; (SOT137A); SOT137-1; 1996 Oct 29.

BLOCK DIAGRAM

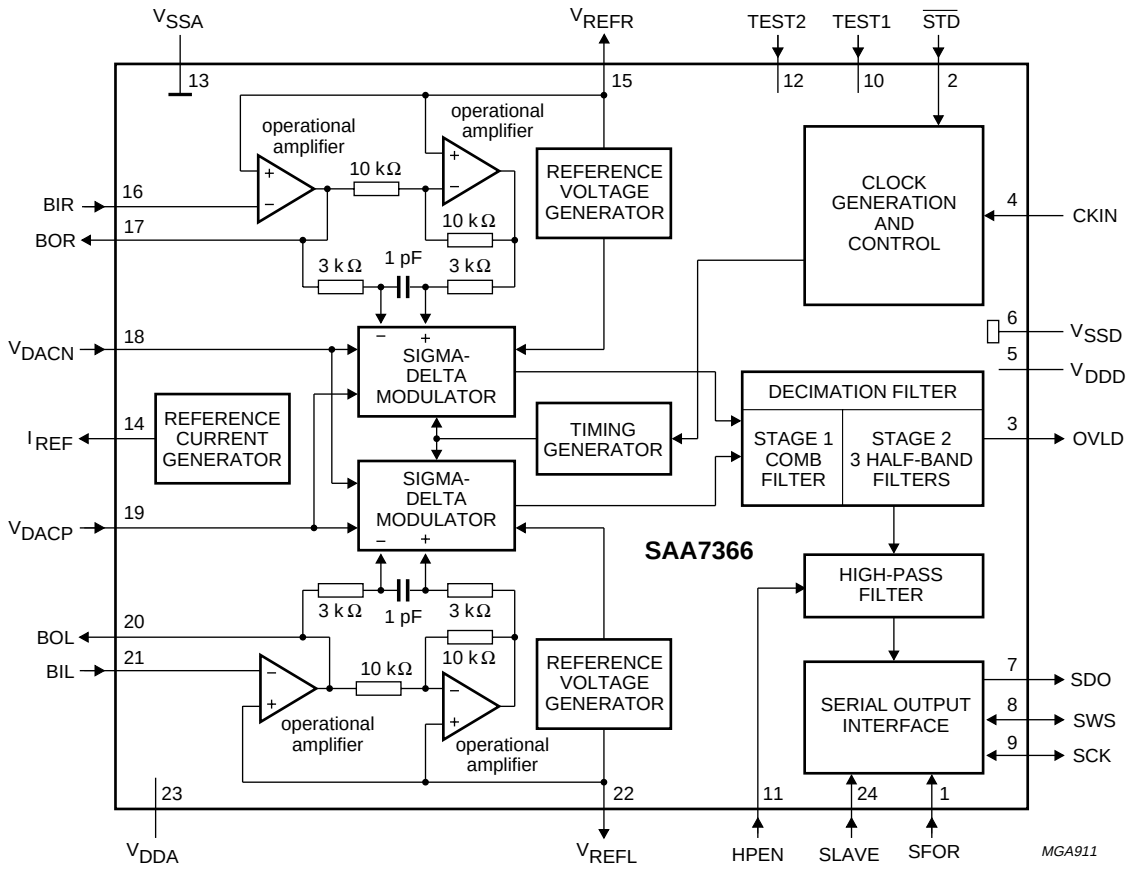


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SFOR	1	Serial interface output format select. Output format is selected as follows: SFOR HIGH = Format 1; SFOR LOW = Format 2.
$\overline{STD}$	2	Standby mode input (active LOW).
OVLD	3	Overload indication output. This pin indicates whether the internal digital signal is within 1 dB of maximum. In standby mode this output is high impedance.
CKIN	4	System clock input.
V_{DDD}	5	Supply for the digital section (3.4 to 5.5 V).
V_{SSD}	6	Ground supply for the digital section.
SDO	7	Serial interface data output. In standby mode this output is high impedance.
SWS	8	Serial interface word select signal. In master mode this pin outputs the serial interface word select signal. In slave mode this pin is the word select input to the serial interface. In standby mode this pin is always an input (high impedance).
SCK	9	Serial interface clock. In master mode this pin outputs the serial interface bit clock. In slave mode this pin is the input for the external bit clock. In standby mode this output is high impedance.
TEST1	10	Test input 1. This pin should be left open-circuit.
HPEN	11	High-pass filter enable input. (HPEN HIGH = enabled). If unconnected this pin defaults HIGH.
TEST2	12	Test input 2. This pin should be left open-circuit.
V_{SSA}	13	Ground supply for the analog section.
I_{REF}	14	Current reference output node.
V_{REFR}	15	$\frac{1}{2}V_{DDA}$ reference generator output for the right channel analog section.
BIR	16	Buffer operational amplifier inverting input for right channel.
BOR	17	Buffer operational amplifier output for right channel.
V_{DACN}	18	Negative 1-bit DAC reference voltage input, connected to 0 V.
V_{DACP}	19	Positive 1-bit DAC reference voltage input, connected to +5 V.
BOL	20	Buffer operational amplifier output for left channel.
BIL	21	Buffer operational amplifier inverting input for left channel.
V_{REFL}	22	$\frac{1}{2}V_{DDA}$ reference generator output for the left channel analog section.
V_{DDA}	23	Supply for the analog section.
SLAVE	24	Serial interface operating output mode master/slave select as follows: HIGH = slave mode; LOW = master mode. If unconnected the pin will default LOW.

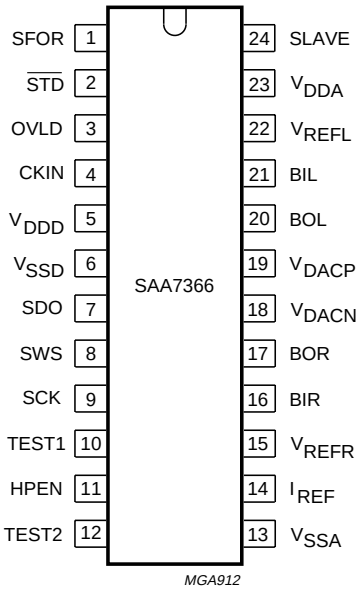


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The SAA7366 is a bitstream conversion CMOS ADC for digital audio systems. The conversion is achieved using a third order Sigma-Delta modulator (SDM), operating at 128 times the output sample frequency (f_s). The high oversampling ratio greatly simplifies the design of the analog input anti-alias filter. In most cases the internal buffer operational amplifier, configured as a low-pass filter will suffice. The 1-bit code from the Sigma-Delta modulator is filtered and down-sampled (decimated) to $1f_s$ in two stages of filtering. An optional high-pass filter is provided to remove DC, if required. The device has been designed with ease of use, low board area and low application costs in mind.

Clock frequency

The external clock, input on pin CKIN, operates at 256 times f_s, which can range from 18 kHz to 53 kHz.

Input buffer

Two input buffers are provided, one for each channel, for signal amplitude matching, signal buffering and anti-alias filter purposes. These are configured for inverting use. Access is provided by pins BIL, BIR (inverting inputs) and BOL, BOR (outputs) for left and right channels respectively. By the choice of feedback component values, the application signal amplitude can be matched to the requirements of the ADC. Typically the operational amplifiers are configured as low-pass filters with a gain of 1 and a pole at approximately $5f_s$.

Remark: The complete ADC is non-inverting. Hence a positive DC input (referenced to V_{ref}) will yield a positive digital output.

Input level

The overall system gain is proportional V_{DDA}, or more accurately $\{V(V_{DACP}) - V(V_{DACN})\}$. For convenience the ADC input signal amplitude is defined as that amplitude seen on BOL or BOR, the operational amplifier outputs (i.e. the input to the Sigma-Delta modulator). Also, the 0 dB input level is defined as that which provides a –1 dB (actually –1.08 dB) digital output, relative to full-scale swing. This offset provides headroom to accommodate small random DC offsets without causing the digital output to clip.

Hence:

$$V_I(0\ dB) = \frac{V(V_{DACP}) - V(V_{DACN})}{5} = V\ (RMS)$$

The user of the IC should ensure, that when all sources of signal amplitude variation are taken into account, the maximum input signal should conform to the 0 dB level. If not, clipping may occur. In the event that the maximum signal level cannot be pre-determined, e.g. a live microphone input, the average signal level should be set at –10 to –20 dB down. The exact value will depend on the application and the balance between head room and operating signal-to-noise ratio.

Behaviour during overload

As defined earlier the maximum input level for normal operation is 0 dB. If the input level exceeds this value clipping may occur. Infringements are limited to the maximum permitted positive or negative values, $2^{17} - 1$ or -2^{17} respectively. If the high-pass filter has been enabled the clipped output samples may have non-maximum values due to the removal of the DC content. Input signals in the range of 0 to 1 dB may or may not be clipped depending on the values of DC dither and small random offsets in the analog circuitry.

When using the recommended application circuitry, clipping will initially be observed on negative peaks due to the use of negative DC dither.

The maximum level of overload that can be safely tolerated is application circuit dependent. In the case of the

recommended circuit the following applies: the inverting operational amplifier inputs BIL/BIR are protected from excessive voltages (currents) by diodes to V_{DDA} and V_{SSA}. These have absolute maximum ratings of $I_{IK} = \pm 20$ mA, with a safe practical limit of ±2 mA. Given the input resistor of 10 kΩ, ±2 mA diode current and the operation of the operational amplifier a maximum signal (applied to the input resistor) of ±30 V can be handled safely. This level represents an overload of 26 dB.

During overload the in-band portion of the waveform will be correctly converted. The out-of-band portion will be limited as detailed above.

Sigma-Delta modulator

The SAA7366 has two third order Sigma-Delta modulators with a quantization noise floor of approximately −104 dB. The scaling of the feedback has been optimized for stable operation even during overload. Thus with a maximum signal swing of 0 V to V_{DDA} on the input the digital output remains well behaved, i.e. it does not burst into random oscillation. During overload the output is simply a clipped version of the input. The gain of this stage is −4.95 dB.

Decimation filter

Decimation from $128f_s$ is performed in two stages. The first stage is a comb filter, which decimates from 128 to $8f_s$. The second stage, consists of 3 half-band filters, each decimating by a factor of 2.

The overall characteristics are given in Table 1.

Table 1 Overall filter characteristics.

ITEM	CONDITION	VALUE (dB)
Pass band ripple	0 to $0.45f_s$ Hz	±0.1
	0.45 to $0.47f_s$	−0.5
Stop band	$>0.55f_s$	−60
Dynamic range	0 to $0.42f_s$	110
Gain	DC	3.87

High-pass filter

An optional high-pass filter is provided to remove unwanted DC components. The operation is selected when HPEN is HIGH. The filter has the characteristics given in Table 2.

Table 2 High-pass filter characteristics.

ITEM	CONDITION	VALUE (dB)
Pass band ripple		none
Pass band gain		0
Droop	at $0.00045f_s$	0.029
Attenuation at DC	at $0.0000036f_s$	>40
Dynamic range	0 to $0.45f_s$	116

Serial interface

The serial interface provides 2 formats in both master and slave modes (see Figs 3 and 4). In both modes the interface provides up to 18 significant bits of output data per channel.

During standby mode ($\overline{STD}$ = LOW) all interface pins are in their high-impedance state. On recovery from standby the serial data output SDO is held LOW until valid data is available from the decimation filter. This time depends on whether the high-pass filter is selected or not as follows:

HPEN = 0; $T = 1024/f_s$, T = 21.3 ms when f_s = 48 kHz

HPEN = 1; $T = 8192/f_s$, T = 170.6 ms when f_s = 48 kHz

Overload Detection Indication (OVLD)

The OVLD output is used to indicate whenever the data, in either the left or right channel, is within 1 dB of the maximum possible digital swing. When this condition is detected the OVLD output is forced HIGH for at least $512f_s$ cycles (10.6 ms at f_s = 48 kHz). This time-out is reset for each infringement.

Standby mode ($\overline{STD}$)

The $\overline{STD}$ pin activates a power saving mode when the device function is not required. This pin can also be used as a chip enable, as follows.

On a HIGH-to-LOW transition, of the $\overline{STD}$ pin, the internal control circuitry starts a timed power-down sequence. This takes approximately 32 system clock cycles to complete. Transitions on $\overline{STD}$ which are shorter than 32 clock cycles have an indeterminate effect. However, the device will always recover correctly.

During standby the following occurs:

- The internal logic clock is disabled
- The serial interface pins are forced to high impedance
- The OVLD output is forced LOW
- The analog circuitry is disabled
- The nominal external analog node voltages are maintained by a low-power circuit. This feature ensures a fast recovery from standby mode.

On a LOW-to-HIGH transition the device reverts back to its normal function. This process takes approximately 32 system clock cycles. Before SDO is enabled the output data is forced LOW. SDO remains LOW until good data is available from the decimation filter.

The $\overline{STD}$ pin has a Schmitt-trigger input. A simple power-on reset function can be effected using an external capacitor to V_{SSD} and resistor to V_{DDD}.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	note 1	–0.5	+6.5	V
V_I	DC input voltage		–0.5	+6.5	V
I_{IK}	DC input diode current		–	±20	mA
V_O	DC output voltage		–0.5	V_{DD} + 0.5	V
I_O	DC output source or sink current		–	±20	mA
I_{DDtot}	total DC supply current		–	±0.5	A
I_{SStot}	total DC supply current		–	±0.5	A
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C
V_{es1}	electrostatic handling	note 2	–2000	+2000	V
V_{es2}	electrostatic handling	note 3	–200	+200	V

Notes

1. V_{SSD} and V_{SSA} pins must be externally connected to a common potential.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

V_{DDD} = 3.4 to 5.5 V; V_{DDA} = 4.5 to 5.5 V; T_{amb} = –40 to +85 °C; f_s = 18 to 53 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	f_s = 48 kHz	–	13	–	mA
V_{DDD}	digital supply voltage		3.4	5.0	5.5	V
I_{DDD}	digital supply current	f_s = 48 kHz	–	56	–	mA
P_{tot}	total power consumption	f_s = 48 kHz	–	345	–	mW

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{STD}	standby supply current		–	65	–	µA
P_{STD}	standby power consumption		–	325	–	µW
Digital part: inputs						
SFOR, SLAVE AND HPEN						
V_{IL}	LOW level input voltage	note 1	–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} + 0.5	V
I_{LI}	input leakage current	note 2	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
CLKIN						
V_{IL}	LOW level input voltage		–0.5	–	$+0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	V_{DDD} + 0.5	V
I_{LI}	input leakage current	note 2	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
$\overline{STD}$ (SCHMITT-TRIGGER)						
V_{IL}	LOW level input voltage	note 1	–0.5	–	$+0.4V_{DDD}$	V
V_{IH}	HIGH level input voltage	note 1	2.4	–	V_{DDD} + 0.5	V
ΔV_I	input hysteresis		–	600	–	mV
I_{LI}	input leakage current	note 2	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
Digital part: Input/Outputs						
SWS AND SCK						
V_{IL}	LOW level input voltage	note 1	–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} + 0.5	V
I_{LI}	leakage current in 3-state	note 2	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_O = –400 µA; note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 µA; note 1	2.4	–	–	V
C_L	output load capacitance		–	–	50	pF
Digital part: Outputs						
OVLD						
V_{OL}	LOW level output voltage	I_O = –400 µA; note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 µA; note 1	2.4	–	–	V
C_L	output load capacitance		–	–	50	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDO						
V_{OL}	LOW level output voltage	I_O = –400 μA; note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 μA; note 1	2.4	–	–	V
I_{LI}	leakage current in 3-state	note 2	–10	–	+10	μA
C_L	output load capacitance		–	–	50	pF
Digital part: timing						
CKIN						
t_r	clock input rise time		–	–	10	ns
t_f	clock input fall time		–	–	10	ns
f_i	clock input frequency	note 3	4.608	12.288	13.568	MHz
msr	mark-to-space ratio	$f_s > 32$ kHz	40	–	60	%
		$f_s \leq 32$ kHz	30	–	70	%
Serial interface master and slave modes (see Figs 5, 6 and 7)						
SCK						
t_r	clock rise time	note 4	–	–	50	ns
t_f	clock fall time	note 4	–	–	50	ns
t_L	clock LOW time	T = 1/64f_s	0.40T	–	0.60T	
t_H	clock HIGH time	T = 1/64f_s	0.40T	–	0.60T	
f_{clk}	clock frequency	master mode	64f_s	64f_s	64f_s	
		slave mode	–	–	64f_s	
t_{idle}	burst clock idle time	slave mode; T = 1/f_s	0	–	0.05T	
SWS						
t_r	word select rise time	note 4	–	–	50	ns
t_f	word select fall time	note 4	–	–	50	ns
t_{wL}	word select LOW time	T = 1/f_s	0.45T	0.50T	0.55T	
t_{wH}	word select HIGH time	T = 1/f_s	0.45T	0.50T	0.55T	
f_{wc}	word select frequency		1f_s	1f_s	1f_s	
t_d	word select delay from SCK	master mode	–50	–	+50	ns
t_d	word select delay from SCK	slave mode	50	–	–	ns
t_{su}	word select set-up time to SCK	slave mode	150	–	–	ns
SDO						
t_h	data output hold time		100	–	–	ns
t_{su}	data output set-up time		100	–	–	ns
t_r	data output rise time	note 4	–	–	50	ns
t_f	data output fall time	note 4	–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog part (V_{DDD} = V_{DDA} = 5 V; T_{amb} = 25 °C; f_s = 48 kHz)						
VOLTAGE REFERENCE: V_{REFL} AND V_{REFR}						
V_O	output voltage		$0.475V_{DDA}$	$0.5V_{DDA}$	$0.525V_{DDA}$	V
Z_n	DC impedance	normal mode	–	750	–	Ω
Z_s	DC impedance	standby mode	–	100	–	kΩ
CURRENT REFERENCE: I_{REF}						
V_O	output voltage		–	$0.5V_{DDA}$	–	V
I_O	output current	R = 33 kΩ	–	76	–	μA
DAC REFERENCE: V_{DACN}						
V_I	input voltage		–	V_{SSA}	–	V
V_{DACP}						
V_I	input voltage		–	V_{DDA}	–	V
BUFFER OPERATIONAL AMPLIFIERS: BIL, BOL, BIR AND BOR						
V_{offset}	input offset voltage		–	$< \pm 10$	–	mV
R_{Lmax}	maximum load resistance; (drive capability)	decoupled to V_{REF}	–	10	–	kΩ
Z_O	output impedance		–	100	–	Ω
THD + N	total harmonic distortion plus noise	f = 0 to 20 kHz	–	–85	–	dB
ADC PERFORMANCE; NOTE 5						
t_{gd}	group delay	$T = 1/f_s$	tbf	–	tbf	μs
α_{sb}	stop band attenuation	$f > 0.546f_s$	60	–	–	dB
DR	dynamic range	note 6	90	–	–	dB
THD + N	total harmonic distortion plus noise	note 7	–	–	–80	dB
S/N	signal-to-noise ratio	A-weighted	–	tbf	–	dB
α_{cs}	channel separation	note 8	–	tbf	–	dB
G	gain	note 9	–1.2	–1	–0.8	dB

Notes

1. Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
2. I_{LImin} and I_{LOmin} measured at V_I = 0 V; I_{LImax} and I_{LOmax} measured at $V_I = V_{DDD}$.
3. f_i is a multiple (×256) of the system sampling frequency (f_s) which can vary between 18 kHz and 53 kHz.
4. C_L = 50 pF (valid for master mode only).
5. Device measured with external components shown in recommended application diagram Fig.8.
6. Input is 1 kHz and –60 dB.
7. Input is 1 kHz and 0 dB.
8. Measured by applying a 1 kHz, 0 dB signal to one channel and monitoring the level of 1 kHz (fundamental) on the other channel.
9. See also Section “Input level” of Chapter “Functional description”; valid for left or right channel.

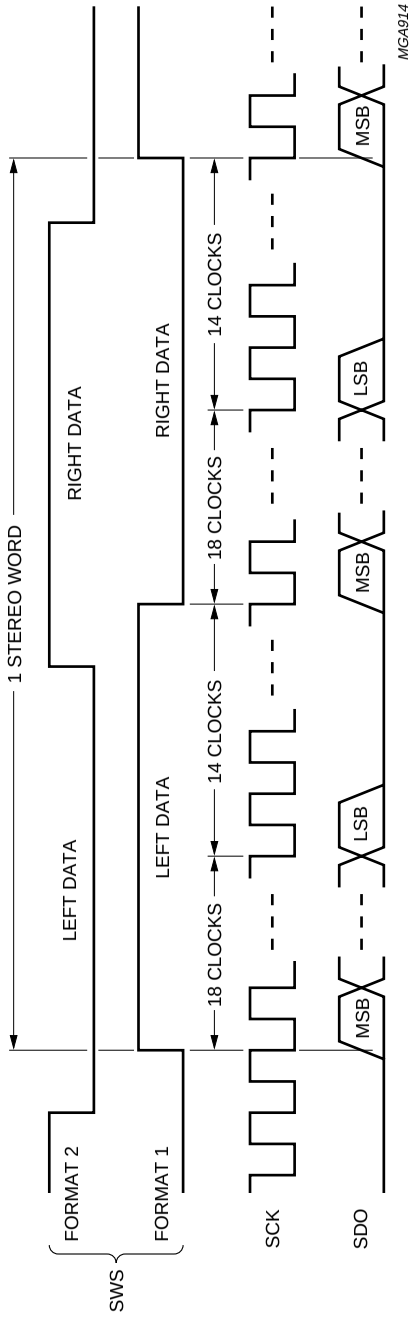


Fig.3 Serial interface master mode format.

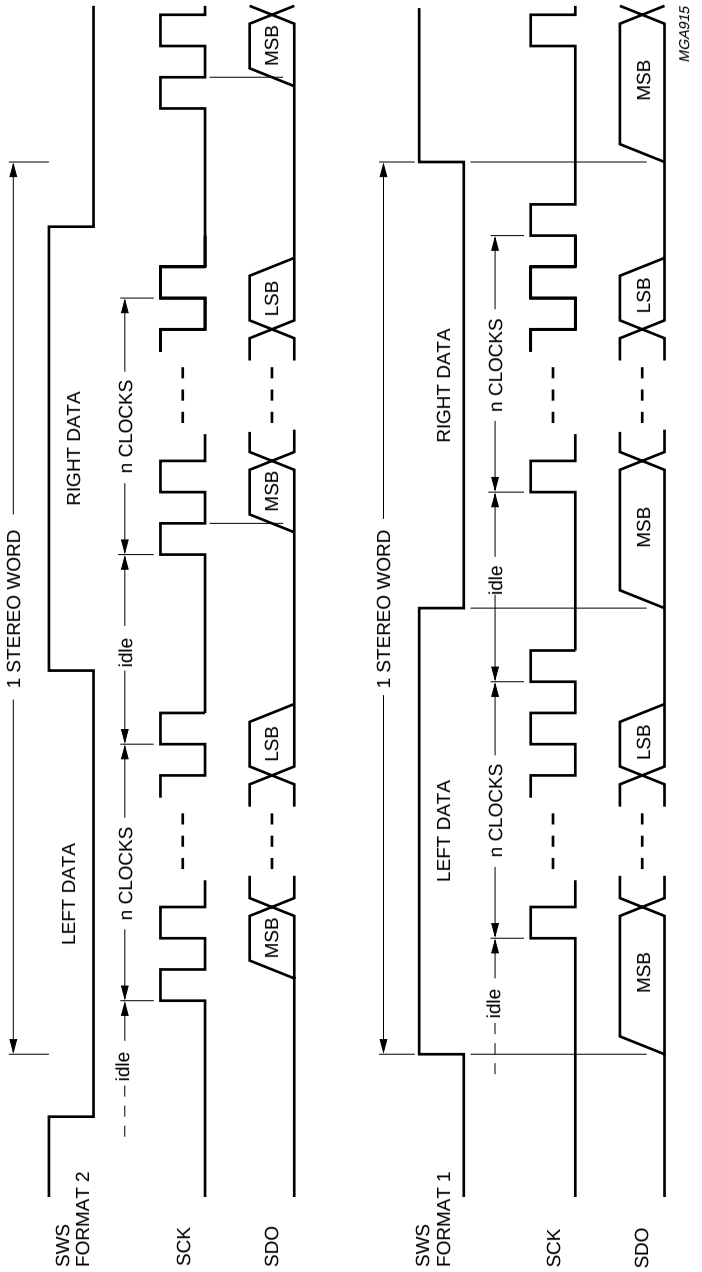


Fig.4 Serial interface slave mode formats.

1 < n < 33.
Up to 18 significant bits are available.

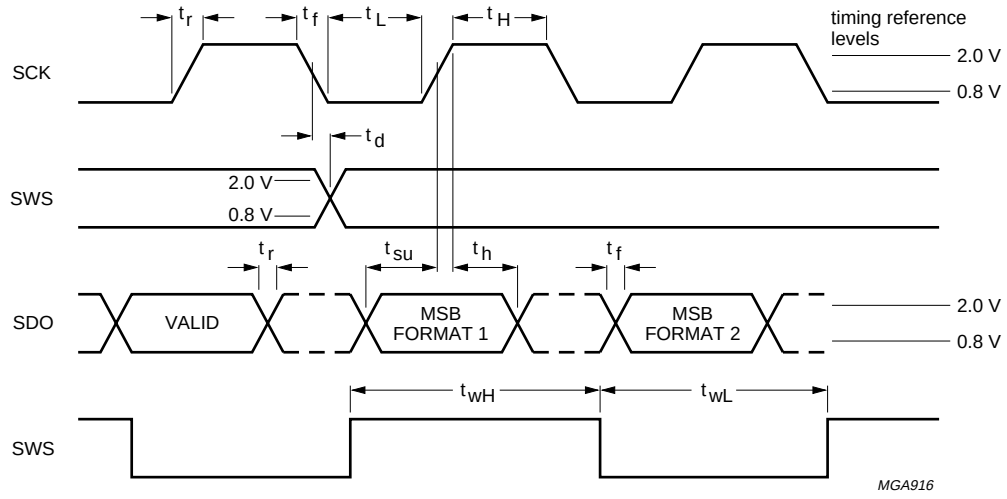


Fig.5 Serial interface master mode timing.

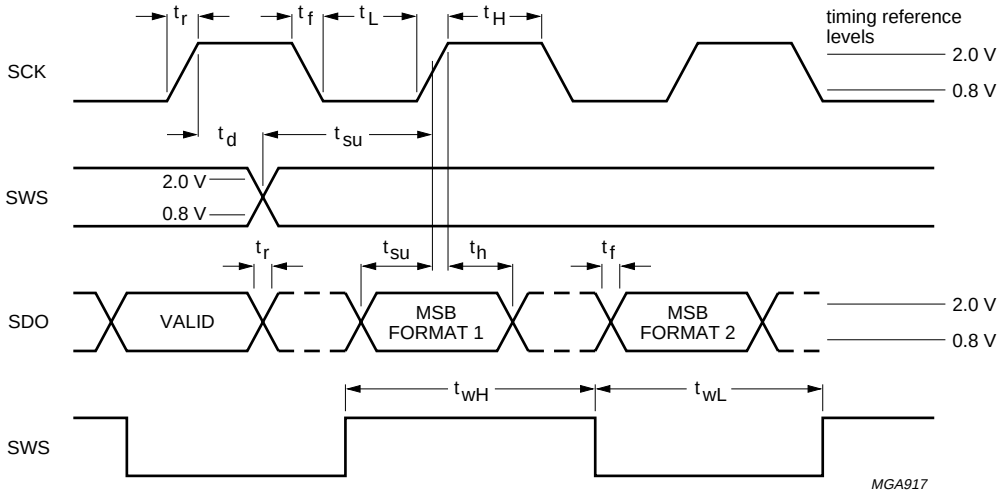


Fig.6 Serial interface slave mode timing.

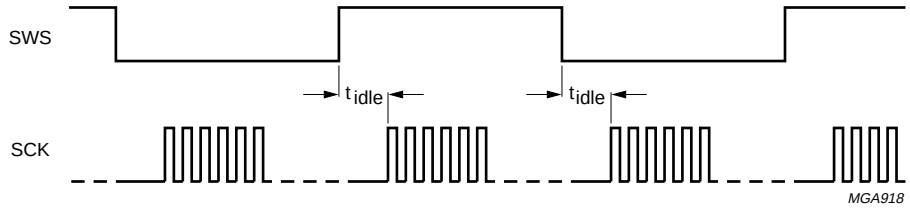
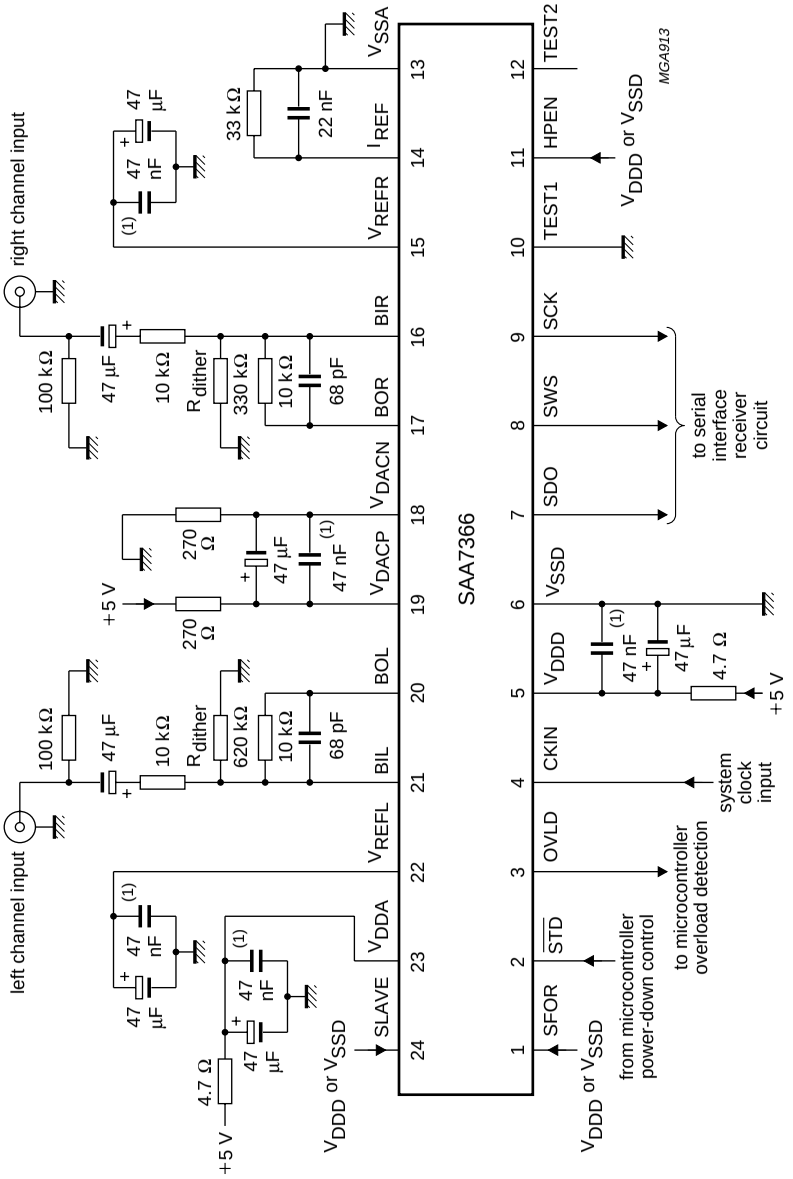


Fig.7 Serial interface slave mode burst clock.

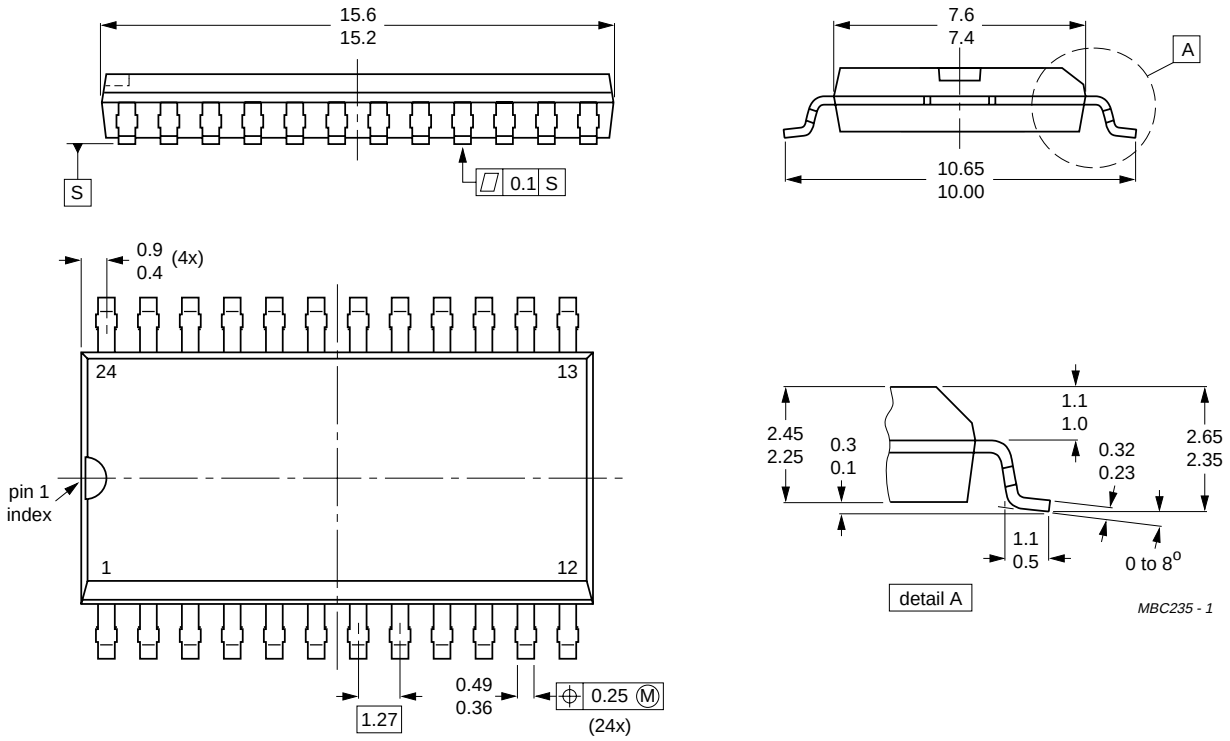
APPLICATION INFORMATION



(1) These capacitors should preferably be surface mounted components located as close as possible to the device pins.

Fig.8 Application circuit.

PACKAGE OUTLINE



Dimensions in mm.

Fig.9 Plastic SOL, 24-pin (SO24L; SOT137A).

SOLDERING

Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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