## OVERVIEW

The SM5840FS/FP is an 8-times oversampling digital filter for digital audio, fabricated using NPC's Moly-Gate® CMOS process. It is intended for use in CD and PCM playback systems.

The SM5840FS/FP features selectable digital deemphasis, attenuation, mute and noise shaping functions. The serial data format consists of 16- or 18-bit input words, supporting the Philips IIS standard, and 18- or 20-bit output words in 2s complement form, supporting interface to a wide range of D/A converters.

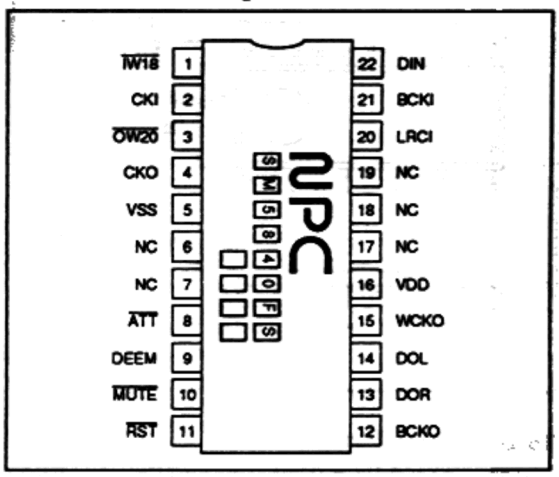
The SM5840FS/FP operates from a 5 V supply and is available in 22-pin SOPs and 18-pin DIPs.

## FEATURES

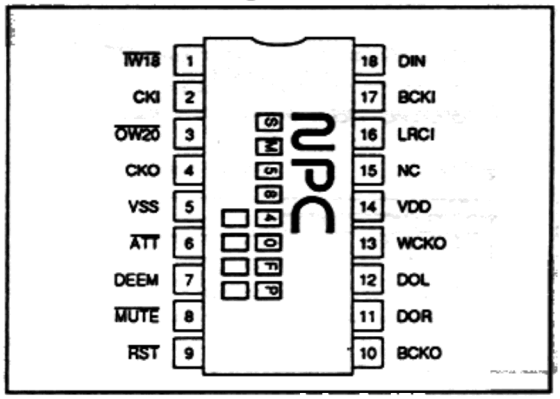
- Two channel 8-times oversampling digital filter
- Three-stage interpolation filters, consisting of 69-tap, 13-tap and 9-tap FIR filters
- IIR deemphasis filter for accurate gain and phase response
- Noise shaper
- 256fs system clock
- 19 × 14-bit multiplier/24-bit accumulator
- Digital attenuator
- Less than ±0.03 dB passband ripple
- Greater than 55 dB stopband attenuation
- Linear phase (no group delay)
- 16- or 18-bit serial input data
- 18- or 20-bit serial output data
- TTL-compatible inputs and outputs
- Moly-Gate® CMOS process
- 5 V supply
- 22-pin SOP and 18-pin DIP

## PINOUTS

22-pin SOP



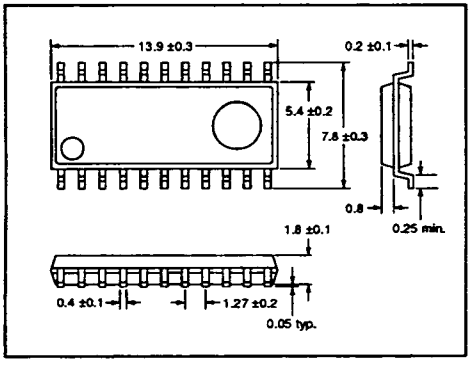

18-pin DIP



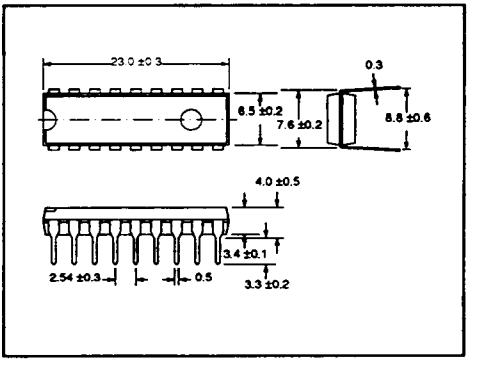
## PACKAGE DIMENSIONS

Unit: mm

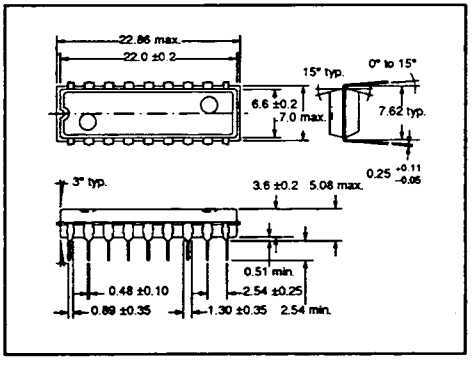
### 22-pin SOP



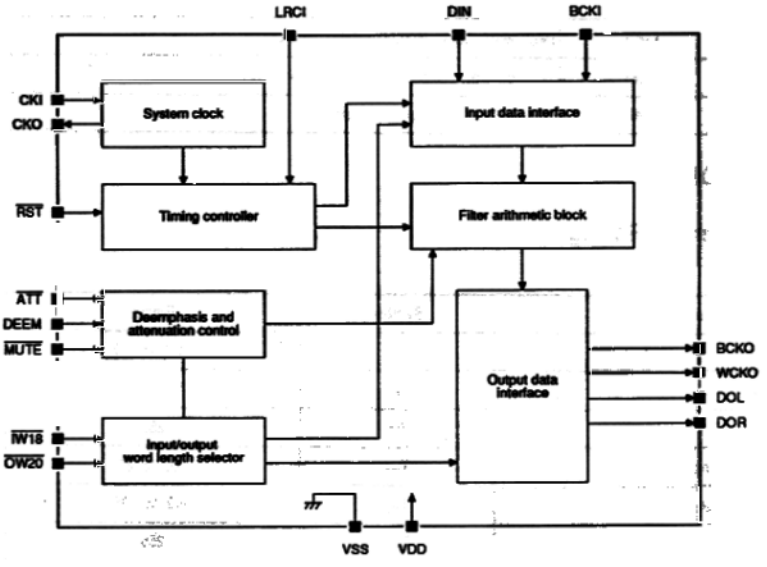

### 18-pin DIP (Type B)




### 18-pin DIP (Type A)



## BLOCK DIAGRAM




## PIN DESCRIPTION

| Number | | Name | Description |
|---|---|---|---|
| SOP | DIP | | |
| 1 | 1 | $\overline{IW18}$ | Input word length select input. 18 bits when LOW and 16 bits when HIGH. Internal pull-up resistor |
| 2 | 2 | CKI | System clock input |
| 3 | 3 | $\overline{OW20}$ | Output word length select input. 20 bits when LOW and 18 bits when HIGH. |
| 4 | 4 | CKO | Buffered, system clock output |
| 5 | 5 | VSS | Ground |
| 6 | – | NC | No connection |
| 7 | – | NC | No connection |
| 8 | 6 | $\overline{ATT}$ | Attenuation enable input. OFF when HIGH and ON when LOW. Internal pull-up resistor |
| 9 | 7 | DEEM | Deemphasis enable input. OFF when LOW and ON when HIGH. Internal pull-up resistor |
| 10 | 8 | $\overline{MUTE}$ | Soft mute enable input. OFF when HIGH and ON when LOW. Internal pull-up resistor |
| 11 | 9 | $\overline{RST}$ | Device reset input. Internal pull-up resistor |
| 12 | 10 | BCKO | Output bit clock |
| 13 | 11 | DOR | Right-channel data output |
| 14 | 12 | DOL | Left-channel data output |
| 15 | 13 | WCKO | Output word clock |
| 16 | 14 | VDD | 5 V supply |
| 17 | – | NC | No connection |
| 18 | – | NC | No connection |
| 19 | 15 | NC | No connection |

| Number | | Name | Description |
|---|---|---|---|
| SOP | DIP | | |
| 20 | 16 | LRCI | Input word clock. Internal pull-up resistor |
| 21 | 17 | BCKI | Input bit clock. Internal pull-up resistor |
| 22 | 18 | DIN | Input data. Internal pull-up resistor |

# SPECIFICATIONS

## Absolute Maximum Ratings

$V_{SS}$ = 0 V

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | $V_{DD}$ | −0.3 to 7.0 | V |
| Input voltage range | $V_I$ | −0.3 to $V_{DD}$ + 0.3 | V |
| Power dissipation | $P_D$ | 250 | mW |
| Operating temperature range | $T_{opr}$ | −20 to 80 | deg. C |
| Storage temperature range | $T_{stg}$ | −40 to 125 | deg. C |
| Soldering temperature | $T_{SLD}$ | 255 | deg. C |
| Soldering time | $t_{SLD}$ | 10 | s |

## Recommended Operating Conditions

$V_{SS}$ = 0 V, $T_a$ = 25 deg. C

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD}$ | 5.0 | V |
| Supply voltage range | $V_{DD}$ | 4.5 to 5.5 | V |

## DC Electrical Characteristics

$V_{DD}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V, $T_a$ = −20 to 80 deg. C unless otherwise noted

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Supply current | $I_{DD}$ | $V_{DD}$ = 5.0 V, $f_{SYS}$ = 256fs = 13 MHz, no load | – | – | 40 | mA |
| CKI and $\overline{OW20}$ LOW-level input voltage | $V_{IL1}$ | | – | – | 0.3$V_{DD}$ | V |
| CKI and $\overline{OW20}$ HIGH-level input voltage | $V_{IH1}$ | | 0.7$V_{DD}$ | – | – | V |
| DEEM, $\overline{ATT}$, $\overline{MUTE}$, $\overline{IW18}$, BCKI, DIN, LRCI and $\overline{RST}$ LOW-level input voltage | $V_{IL2}$ | | – | – | 0.5 | V |
| DEEM, $\overline{ATT}$, $\overline{MUTE}$, $\overline{IW18}$, BCKI, DIN, LRCI and $\overline{RST}$ HIGH-level input voltage | $V_{IH2}$ | | 2.4 | – | – | V |
| CKI clock input voltage | $V_{INAC}$ | AC-coupled, sine-wave input | 0.3$V_{DD}$ | – | – | $V_{P-P}$ |

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| DOL, DOR, BCKO, CKO and WCKO LOW-level output voltage | $V_{OL}$ | $I_{OL}$ = 1.6 mA | – | – | 0.4 | V |
| DOL, DOR, BCKO, CKO and WCKO HIGH-level output voltage | $V_{OH}$ | $I_{OH}$ = –0.4 mA | 2.5 | – | – | V |
| CKI LOW-level input current | $I_{IL1}$ | $V_I$ = 0 V | – | 10 | 20 | µA |
| CKI HIGH-level input current | $I_{IH1}$ | $V_I$ = $V_{DD}$ | – | 10 | 20 | µA |
| $\overline{OW20}$ LOW-level input leakage current | $I_{LL}$ | $V_I$ = 0 V | – | – | 1.0 | µA |
| $\overline{ATT}$, $\overline{IW18}$, $\overline{OW20}$, DEEM, $\overline{MUTE}$, LRCI, DIN, BCKI and $\overline{RST}$ HIGH-level input leakage current | $I_{LH}$ | $V_I$ = $V_{DD}$ | – | – | 1.0 | µA |
| DEEM, $\overline{ATT}$, $\overline{MUTE}$, $\overline{IW18}$, $\overline{RST}$, LRCI, DIN, BCKI, and $\overline{RST}$ LOW-level input current | $I_{IL2}$ | $V_I$ = 0 V | – | 10 | 20 | µA |

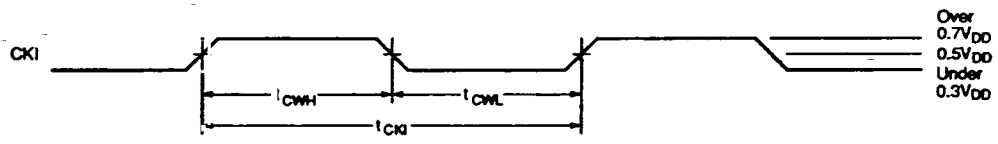
## AC Electrical Characteristics

### System clock

$V_{DD}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V, $T_a$ = –20 to 80 deg. C

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| CKI LOW-level clock pulsewidth | $t_{CWL}$ | 35 | – | 500 | ns |
| CKI HIGH-level clock pulsewidth | $t_{CWH}$ | 35 | – | 500 | ns |
| CKI clock cycle time | $t_{CKI}$ | 76 | – | 1000 | ns |

### System clock timing waveform




### Reset timing

$V_{DD}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V, $T_a$ = –20 to 80 deg. C

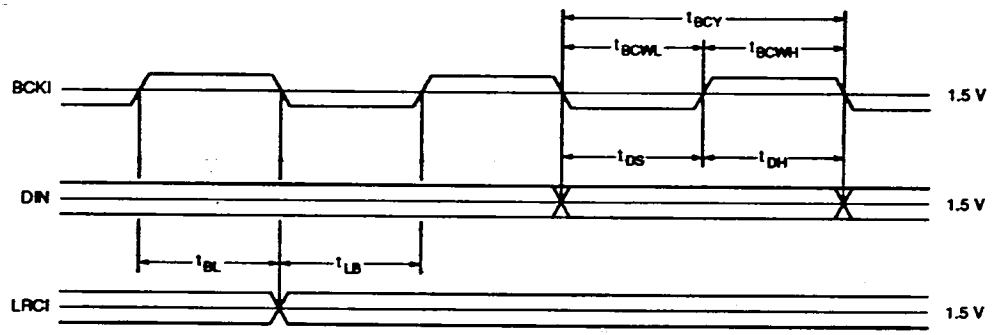
| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| $\overline{RST}$ LOW-level pulsewidth | $t_{RST}$ | At power-on | 1 | – | – | µs |
| | | At other times | 50 | – | – | ns |

## BCKI, DIN, LRCI input timing

$V_{DD}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V, $T_a$ = −20 to 80 deg. C

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| BCKI LOW-level pulsewidth | $t_{BCWL}$ | 50 | – | – | ns |
| BCKI HIGH-level pulsewidth | $t_{BCWH}$ | 50 | – | – | ns |
| BCKI pulse period | $t_{BCY}$ | 100 | – | – | ns |
| DIN setup time | $t_{DS}$ | 50 | – | – | ns |
| DIN hold time | $t_{DH}$ | 50 | – | – | ns |
| Last BCKI rising edge to LRCI edge | $t_{BL}$ | 50 | – | – | ns |
| LRCI edge to first BCKI rising edge | $t_{LB}$ | 50 | – | – | ns |

## BCKI, DIN, LRCI input timing waveform




## $\overline{ATT}$, DEEM, MUTE control input timing

$V_{DD}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V, $T_a$ = −20 to 80 deg. C

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| $\overline{ATT}$, DEEM and MUTE rise time | $t_r$ | – | – | 100 | ns |
| $\overline{ATT}$, DEEM and MUTE fall time | $t_f$ | – | – | 100 | ns |

**Note**

Rise times and fall times are measured between 10% and 90% of $V_{DD}$.

## Output timing

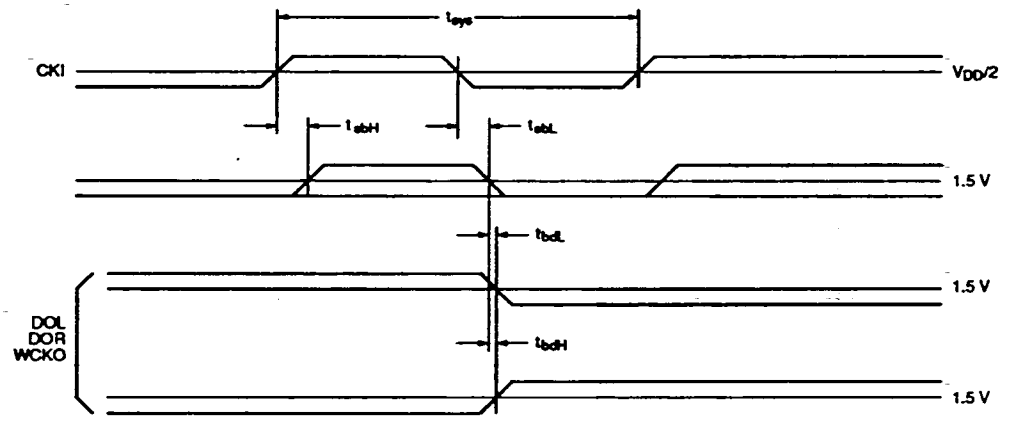
$V_{DD}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V, $T_a$ = −20 to 80 deg. C

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| CKI falling edge to CKO falling edge | $t_{CKO}$ | 7 | – | 30 | ns |
| CKI falling edge to BCKO falling edge | $t_{abL}$ | 10 | – | 60 | ns |
| CKI falling edge to BCKO rising edge | $t_{abH}$ | 10 | – | 60 | ns |
| BCKO falling edge to DOL, DOR or WCKO falling edge | $t_{bdL}$ | 0 | – | 20 | ns |
| BCKO falling edge to DOL, DOR or WCKO rising edge | $t_{bdH}$ | 0 | – | 20 | ns |

**Note**

All measurements with 15 pF capacitive load

### Output timing waveform

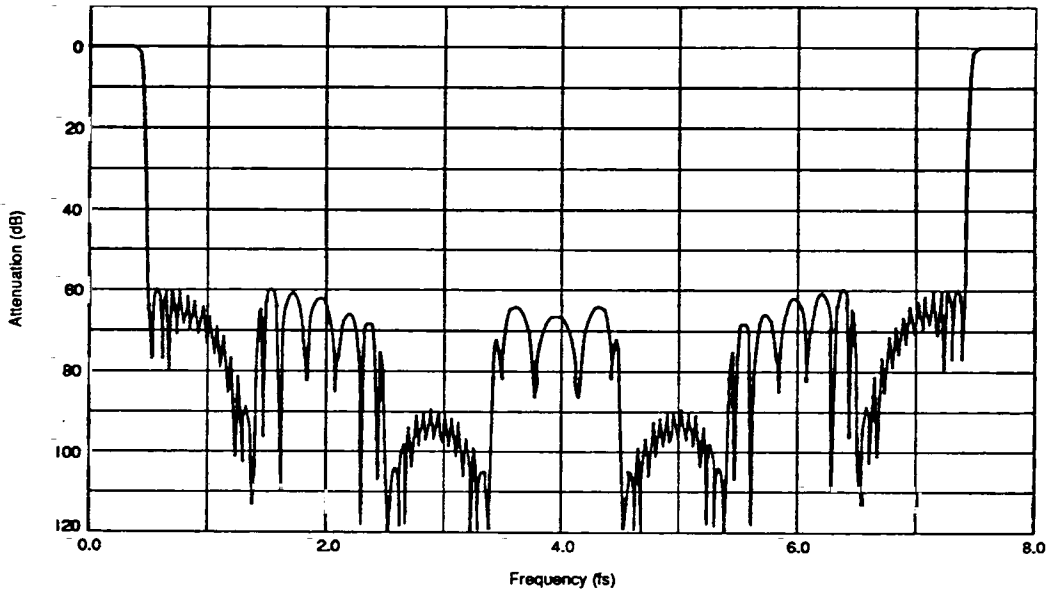



## Filter Characteristics

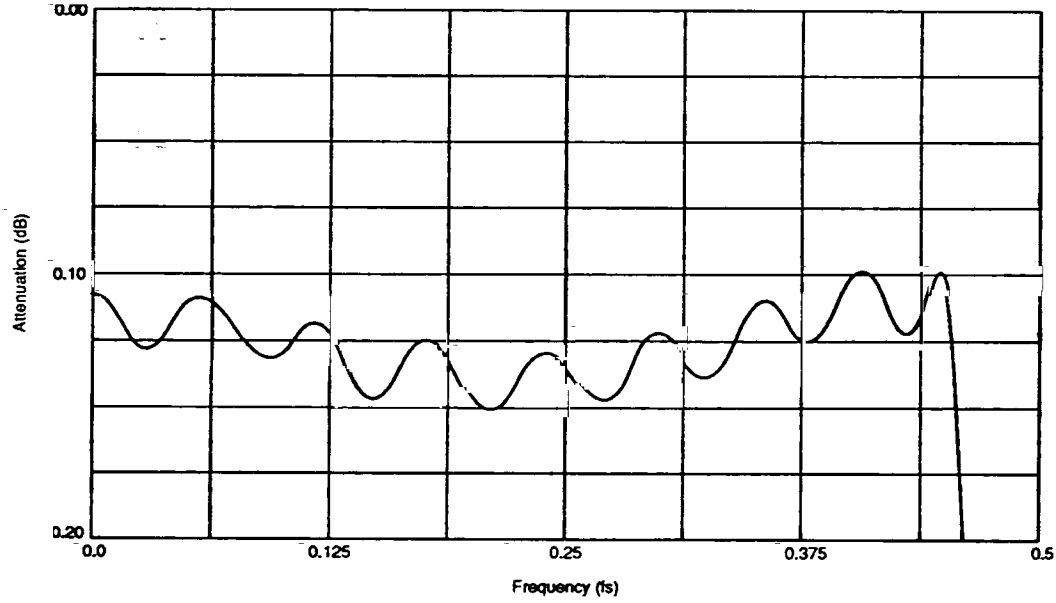
### 8-times oversampling mode

| Parameter | Rating |
|---|---|
| Passband | 0 to 0.4535fs |
| Stopband | 0.5465fs to 7.4535fs |
| Passband attenuation level | 0.125 ±0.03 dB |
| Stopband attenuation | > 55 dB |
| Group delay time | Constant |

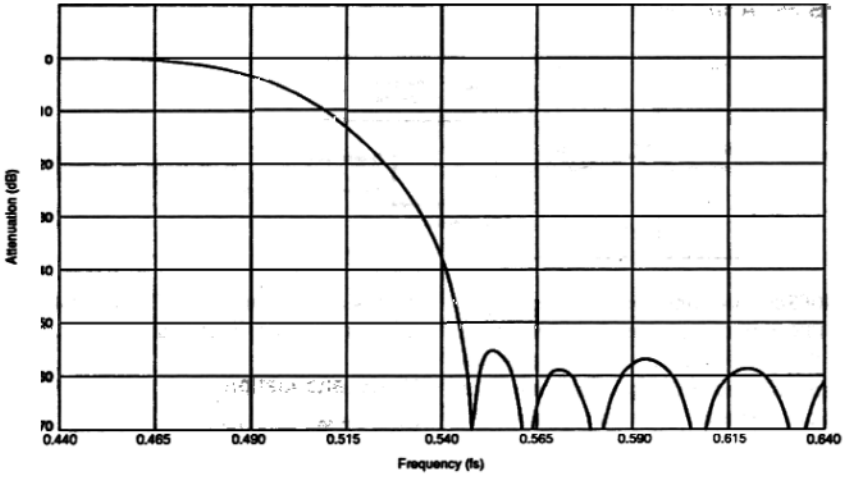
## Frequency characteristic without deemphasis




## Passband characteristic without deemphasis



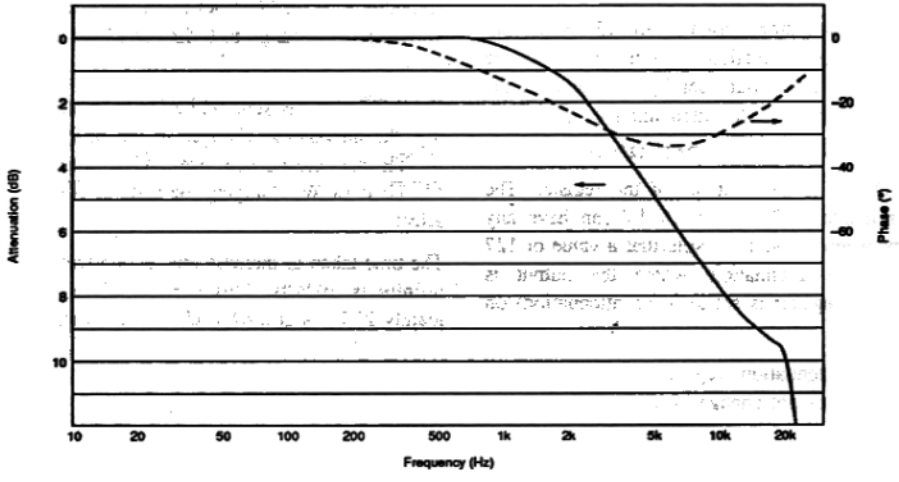
## Transition characteristic without deemphasis




## Deemphasis filter

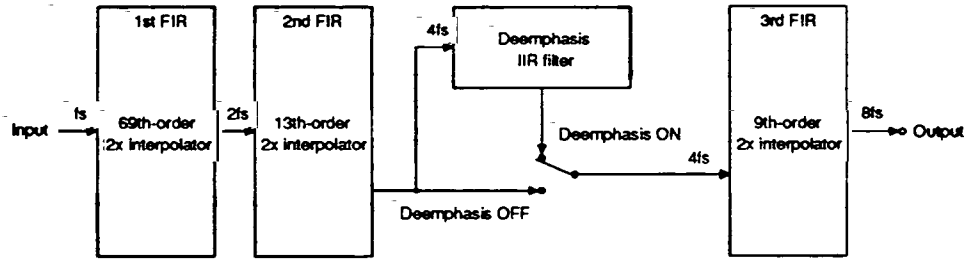
| Parameter | | Rating |
|---|---|---|
| Sampling frequency (fs) | | 44.1 |
| Passband (kHz) | | 0 to 20.0 |
| Deviation from ideal characteristic | Attenuation (dB) | ±0.001 |
| | Phase (θ) | 0 to 1.5° |

## Passband characteristic with deemphasis



# FUNCTIONAL DESCRIPTION

## SM5840FS/FP Arithmetic Block




The SM5840FS/FP performs oversampling using a multi-stage FIR interpolation filter. Each filter stage interpolates the signal by a factor of two, giving an overall interpolation factor of eight. Sampling noise components are attenuated by the interpolation filter to greater than 55 dB in the 0.5465fs to 7.4535fs stopband.

## Digital Deemphasis

The deemphasis filter is in cascade with the oversampling filters. It is implemented using an IIR filter, and reproduces the deemphasis gain and phase characteristics more faithfully than conventional analog deemphasis filters. Deemphasis is enabled when DEEM is HIGH, and disabled when DEEM is LOW.

The deemphasis filter coefficients are designed for use at fs = 44.1 KHz.

## Digital Attenuator

The digital attenuator is used for the 12 dB attenuation and mute functions. Both channels are attenuated by an amount set by the value in the attenuation register. The attenuation is given by

$$\text{Attenuation} = -20 \log_{10}(1 - \text{DATT}/127) \text{ dB}$$

where DATT is the contents of the register. The register length is 7 bits, so DATT can have any value between 0 and 127. Note that a value of 127 gives infinite attenuation, where the output is muted. The register is set to 0 (no attenuation) on reset.

When the attenuation register is changed, the attenuation does not change instantly, but ramps to the new attenuation setting. This prevents unwanted spurious response in the audio output.

### 12 dB attenuation

When $\overline{\text{ATT}}$ goes LOW, DATT ramps smoothly from 0 to 96, causing the attenuation to change from 0 dB to 12 dB. When $\overline{\text{ATT}}$ goes HIGH, DATT ramps smoothly from 96 to 0, causing the attenuation to change from 12 dB to 0 dB.

If $\overline{\text{ATT}}$ changes state while DATT is still changing, the attenuation changes in the new direction.

The time taken to increase attenuation from 0 dB to 12 dB is 768/fs. This corresponds to approximately 17.4 ms at a 44.1 kHz input sampling rate.

### Mute

When $\overline{\text{MUTE}}$ goes LOW, DATT ramps smoothly to 127, causing the attenuation to change to infinity. When $\overline{\text{MUTE}}$ goes HIGH, DATT ramps smoothly to 0 (or 96 if $\overline{\text{ATT}}$ is LOW), causing the attenuation to change to 0 dB (or 12 dB if $\overline{\text{ATT}}$ is LOW).

If $\overline{\text{MUTE}}$ changes state while DATT is still changing, the attenuation changes in the new direction. $\overline{\text{MUTE}}$ has precedence over $\overline{\text{ATT}}$. Therefore, if $\overline{\text{MUTE}}$ is LOW, changing the state of $\overline{\text{ATT}}$ has no affect.

The time taken to increase attenuation from 0 dB to infinity is 1024/fs. This corresponds to approximately 23.2 ms at a 44.1 kHz input sampling rate.

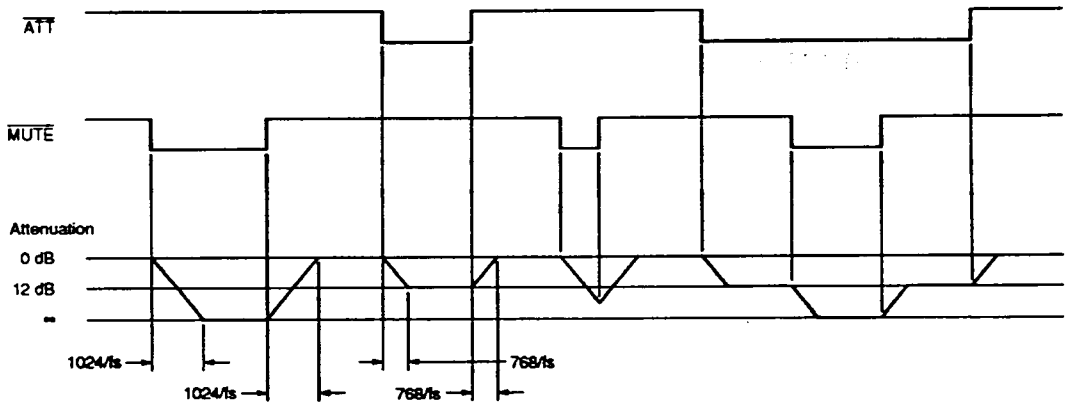



Figure 1. Mute and attenuation timing

## Selectable Input Word Length

When $\overline{IW18}$ is LOW, input word length is 18 bits, and when HIGH, 16 bits.

For 16-bit input source data to the DSP, the DSP can process the data to round it up to 18 bits to reduce the requantization noise in the digital filter.

## Noise Shaper and Selectable Output Word Length

When $\overline{OW20}$ is LOW, output word length is 20 bits, and when HIGH, 18 bits. This enables the SM5840FS/FP to be used with 18- or 20-bit DACs.

The on-chip noise shaper further reduces requantization noise. The noise shaper does not work when 18-bit input and 20-bit output word lengths are selected ($\overline{IW18}$ and $\overline{OW20}$ both LOW).

## System Clock

The system clock is input on CKI and output on CKO. Because the inverter in the CKI input circuit has a feedback resistor, the clock input can either be DC coupled or AC coupled.

Table 1. Clock values

| Clock | Symbol | Value |
|---|---|---|
| CKI input frequency | $f_{CI}$ = (1/$t_{CI}$) | 256fs |
| CKO output frequency | $f_{CO}$ | 256fs |
| Internal system clock period | $T_{SYS}$ | $t_{CI}$ |

**Note**
$t_{CI}$ is the period of CKI.

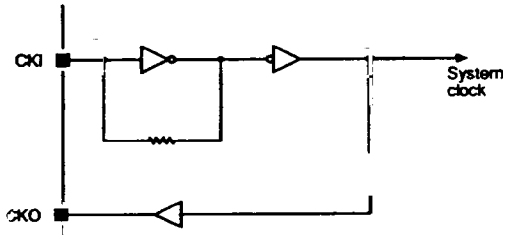



Figure 2. Internal system clock

## Audio Data Input

The SM5840FS/FP can read only 64fs IIS format input data. 32fs IIS format data cannot be read. Serial input data in this format must be 16- or 18-bit, 2s-complement and msb-first. The input word length is selected by $\overline{IW18}$.

The data is input to DIN. Each bit is shifted into an input data shift register on the rising edge of the BCKI bit clock for conversion to parallel data. The contents of the shift registers are latched into the input registers on alternate transitions of the LRCI word clock. Left-channel data is shifted in when LRCI is LOW and right-channel data is shifted in when LRCI is HIGH.

The timing of the input stage is independent of the timing of the arithmetic circuitry. Hence, the phase relationship between the BCKI and LRCI clocks and the system clock does not affect functional operation, provided that the phase relationship remains constant (that is, the frequency ratio of the clocks is constant). This ensures that a certain amount of jitter in the input clock does not affect output signal timing.

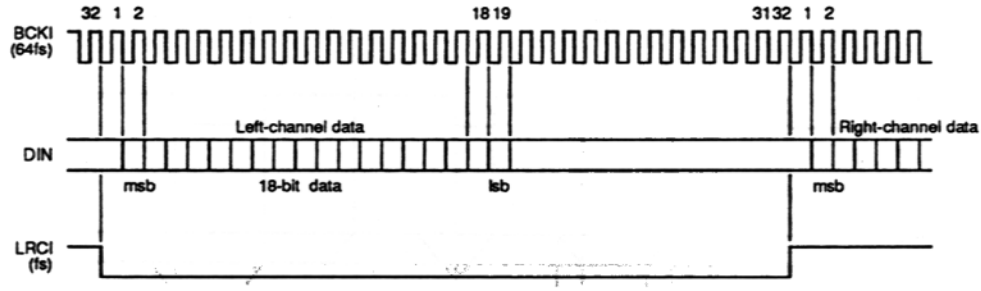



Figure 3. Input timing ($\overline{IW18}$ = LOW)

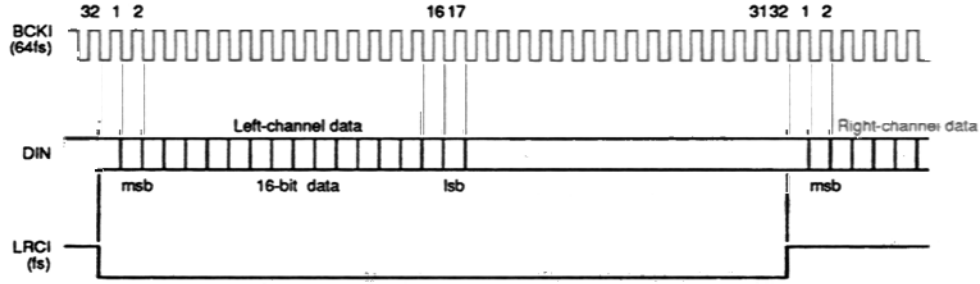



Figure 4. Input timing ($\overline{IW18}$ = HIGH or open)

## Audio Data Output

The audio output data is in bit-serial, 2s complement, msb-first format. The output word length is 18- or 20-bit, as selected by $\overline{OW20}$.

The BCKO output carries the output bit clock, generated within the SM5840FS/FP. The data outputs, DOL and DOR, change on the falling edge of BCKO. The number of bit periods per output word depends on the setting of $\overline{OW20}$ as shown in table 2. Thus, regardless of the number of output bits, the data can be synchronized to the falling edge of WCKO.

Table 2. Output timing

| Parameter | Value |
|---|---|
| Output bit clock rate, $t_B$ | 1/256fs |
| Bit periods per word, $t_{DW}$ | $32t_B$ |

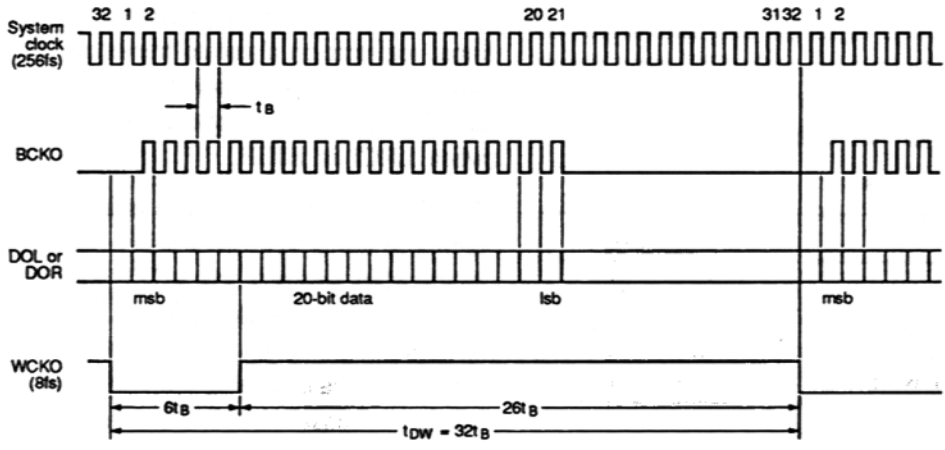



Figure 5. Output timing ($\overline{OW20}$ = LOW)

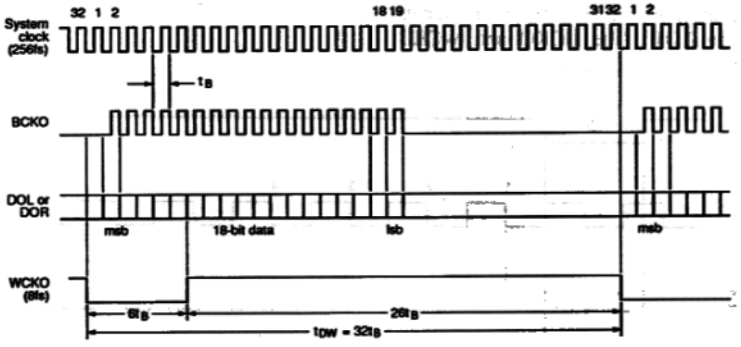



Figure 6. Output timing ($\overline{OW20}$ = HIGH or open)

## System Reset

The SM5840FS/FP must be reset following power-on by applying a LOW-level pulse to the $\overline{RST}$ pin. On the first rising edge of LRCI after $\overline{RST}$ is released, the arithmetic and output timing counters are reset.

A power-on reset can be effected either by a signal from the controlling microprocessor or by connecting a capacitor of approximately 300 pF between $\overline{RST}$ and VSS. Note that in both cases, CKI and LRCI must stabilize before $\overline{RST}$ goes HIGH. A larger capacitor can be used to ensure that this occurs.

The device must also be reset if either LRCI and/or CKI are interrupted or drift apart as shown in figure 7. In this example, NX and NS represent the number of CKI clock periods and LRCI clock periods, respectively, since the first rising edge of LRCI following the rise of $\overline{RST}$.

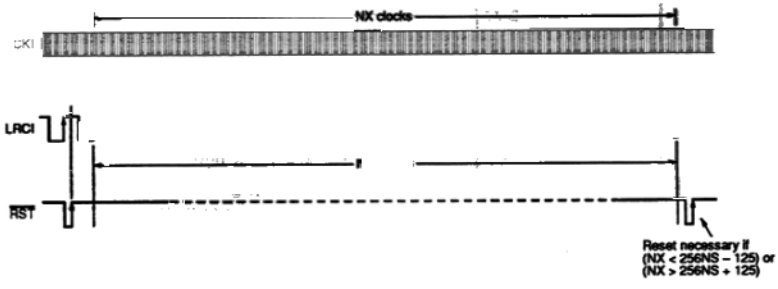



Figure 7. Reset after CKI halt

When $\overline{RST}$ goes LOW, the DOL and DOR outputs immediately go LOW. The BCKO and WCKO outputs do not stop. See figure 8.

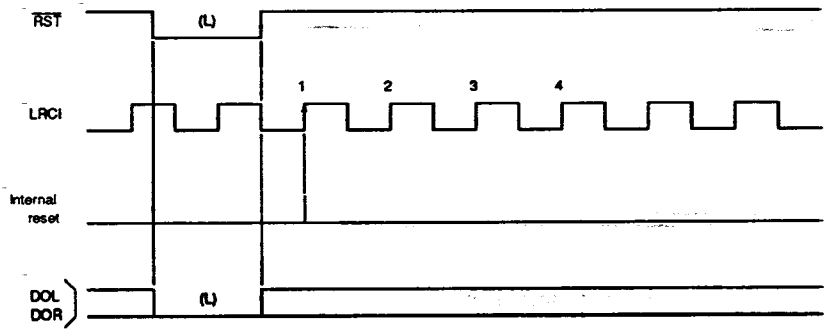
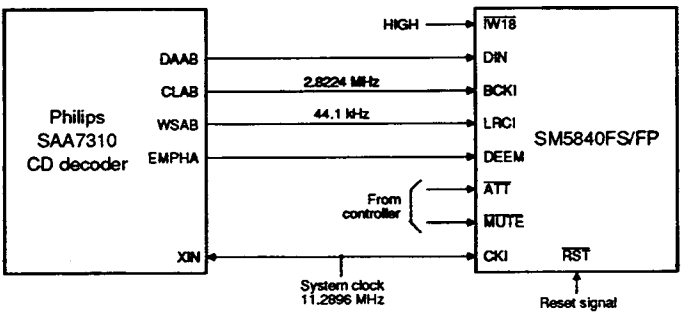



Figure 8. Output timing on reset

## APPLICATION CIRCUITS

These circuits show signal formats and interconnection only. The system designer must also consider the timing relationships.

### 16-bit CD Decoder Interface




### 18-bit DAC Interface