# DATA SHEET

DIGITAL dcc COMPACT CASSETTE

# TDA1318
## DCC read amplifier

Preliminary specification
File under Integrated Circuits, IC01

April 1996

Philips Semiconductors

PHILIPS

# DCC read amplifier TDA1318

## FEATURES

- Differential inputs for a low-power head configuration
- Low-noise current sources for the sense currents of the DCC head
- Reduced power consumption by separate on/off switching of the circuits and sense current of the DCC and CC parts of the IC
- The IC can be used with both the first and second generation DCC digital signal processing ICs
- High-impedance outputs in the OFF state so that the outputs of the ICs can be connected in parallel for dual decks or for decks with electrical auto-reverse heads
- AGC of DCC preamplifiers (can be switched off)
- Possibility of analog audio via DCC preamplifiers (analog via digital readers, ADR mode)
- Single 5 V supply.

## GENERAL DESCRIPTION

The TDA1318 amplifies, filters and multiplexes signals arriving from magneto-resistive thin film heads (MRHs) which are suitable for DCC (Digital Compact Cassette) and CC (Compact Cassette) systems. The device also has current sources to provide sense currents through the DCC-MRHs and two amplifiers for magnetic feedback and biasing.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS[1] | | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | CS | SD | ADR | | | | |
| $V_{DD}$ | supply voltage | – | – | – | 4.5 | 5.0 | 5.5 | V |
| $V_{CCM}$ | supply voltage feedback amplifiers | – | – | – | 4.5 | 5.0 | 5.5 | V |
| $I_{DDDCC}$ | supply current DCC mode (note 2) | 1 | 1 | 0 | – | 31 | 41 | mA |
| $I_{DDDCCadr}$ | supply current DCC mode (ADR) | 1 | 1 | 1 | – | 31 | 41 | mA |
| $I_{DDCC}$ | supply current CC mode | 1 | 0 | 0 | – | 9.7 | 13 | mA |
| $I_{DDCCadr}$ | supply current CC mode (ADR) | 1 | 0 | 1 | – | 17.8 | 24.5 | mA |
| $I_{CCM}$ | supply current feedback amplifiers | 1 | 1 | 1 | – | 8.5 | 12 | mA |
| | | 1 | 0 | 0 | | | | |
| | | 1 | 0 | 1 | | | | |
| $I_{DD}$ | supply current (ADC reference ON) | 0 | 1 | – | – | 1.6 | 2.2 | mA |
| $I_{DD(Q)}$ | total quiescent current in OFF mode | 0 | 0 | – | – | – | 300 | µA |
| $P_{tot}$ | total power dissipation, DCC mode | – | – | – | – | 250 | – | mW |
| $T_{amb}$ | operating ambient temperature | – | – | – | –30 | – | +85 | °C |

**Notes**

1. In the conditions column 0 = LOW; 1 = HIGH.
2. ADR = 1 when pin INL and/or INR is connected to $V_{SS}$.

## ORDERING INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE | | | |
|---|---|---|---|---|
| | PINS | PIN POSITION | MATERIAL | CODE |
| TDA1318H | 44 | QFP44S10[1] | plastic | SOT307-2 |

**Note**

1. When using IR reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocket book"* (order number 9398 510 34011) are followed.

## BLOCK DIAGRAM

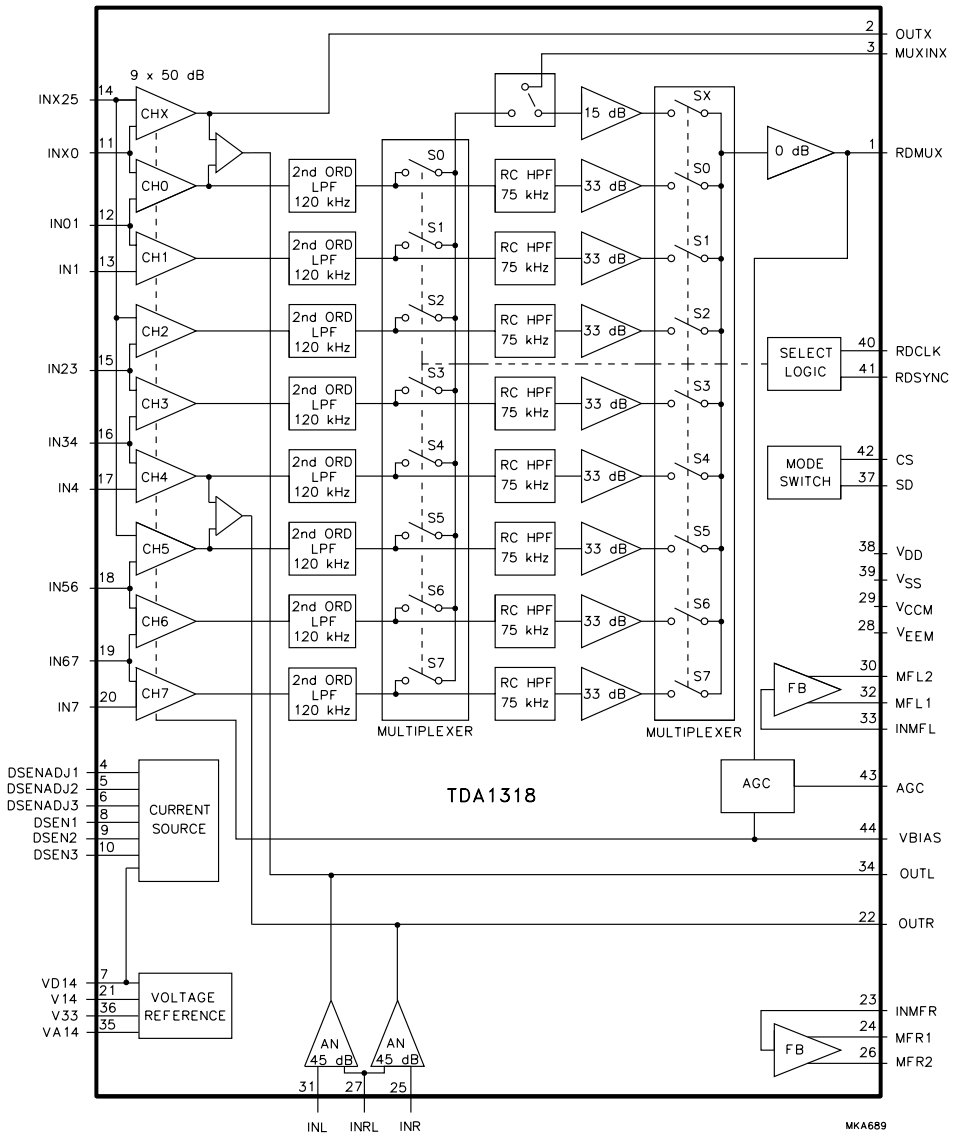



Fig.1 Block diagram.

**PINNING**

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| RDMUX | 1 | output for sampled and multiplexed auxiliary and main data signals |
| OUTX | 2 | auxiliary channel preamplifier output |
| MUXINX | 3 | auxiliary channel multiplexer input |
| DSENADJ1 | 4 | adjustment pin for DCC sense current 1 |
| DSENADJ2 | 5 | adjustment pin for DCC sense current 2 |
| DSENADJ3 | 6 | adjustment pin for DCC sense current 3 |
| VD14 | 7 | reference voltage output DCC sense |
| DSEN1 | 8 | DCC sense current output 1 |
| DSEN2 | 9 | DCC sense current output 2 |
| DSEN3 | 10 | DCC sense current output 3 |
| INX0 | 11 | auxiliary channel input/channel 0 input |
| IN01 | 12 | channels 0 and 1 input |
| IN1 | 13 | channel 1 input |
| INX25 | 14 | channels AUX, 2 and 5 input |
| IN23 | 15 | channels 2 and 3 input |
| IN34 | 16 | channels 3 and 4 input |
| IN4 | 17 | channel 4 input |
| IN56 | 18 | channels 5 and 6 input |
| IN67 | 19 | channels 6 and 7 input |
| IN7 | 20 | channel 7 input |
| V14 | 21 | reference voltage output for DCC/analog inputs |
| OUTR | 22 | right channel analog output |

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| INMFR | 23 | right channel feedback amplifier input |
| MFR1 | 24 | right channel feedback amplifier output 1 |
| INR | 25 | right channel analog input |
| MFR2 | 26 | right channel feedback amplifier output 2 |
| INRL | 27 | right/left channel analog input |
| $V_{EEM}$ | 28 | ground for feedback amplifiers |
| $V_{CCM}$ | 29 | positive supply for feedback amplifiers |
| MFL2 | 30 | left channel feedback amplifier output 2 |
| INL | 31 | left channel analog input |
| MFL1 | 32 | left channel feedback amplifier output 1 |
| INMFL | 33 | left channel feedback amplifier input |
| OUTL | 34 | left channel analog output |
| VA14 | 35 | reference voltage output CC sense |
| V33 | 36 | ADC reference voltage output |
| SD | 37 | select DCC part input |
| $V_{DD}$ | 38 | positive supply voltage |
| $V_{SS}$ | 39 | ground |
| RDCLK | 40 | read clock input |
| RDSYNC | 41 | read sync pulse input |
| CS | 42 | chip select input |
| AGC | 43 | AGC time constant |
| VBIAS | 44 | DCC preamplifier control voltage |

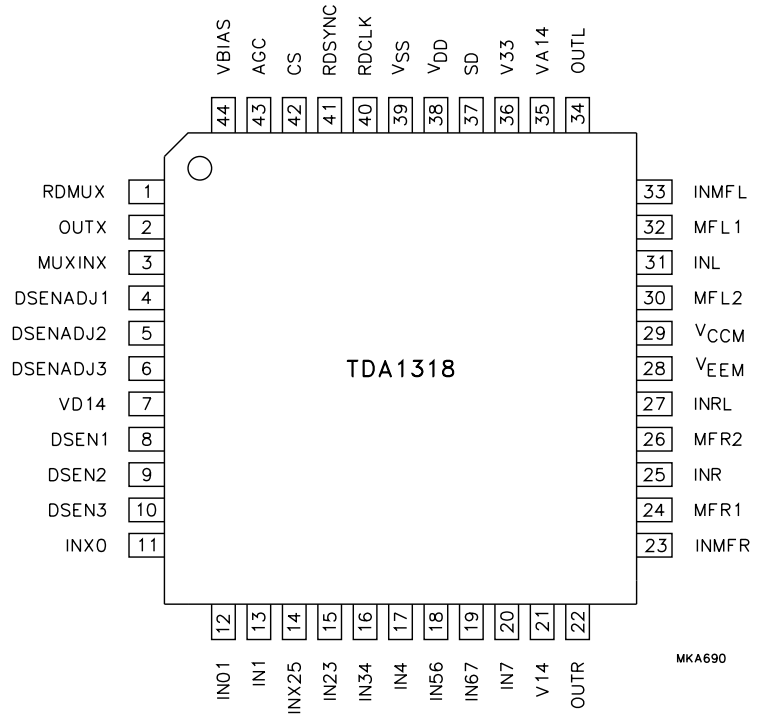



Fig.2 Pin configuration.

## FUNCTIONAL DESCRIPTION

### DCC data amplifiers

For DCC operation the TDA1318 has eight channels for the main data and one channel for the auxiliary data. The eight main data channels have low-noise preamplifiers, pre-equalisation for frequencies from 1 kHz to 50 kHz (1st order high-pass filter, –3 dB point 75 kHz) and low-pass filtering for anti-aliasing (2nd order active, –3 dB point 120 kHz). The auxiliary channel has a preamplifier with a flat frequency response. A continuous output (OUTX) is available for this channel. All inputs are differential and must be AC-coupled to the MRHs. The inputs are internally biased by V14.

### Automatic gain control

The DCC part is equipped with an AGC circuit which diminishes the gain of the DCC preamplifiers when the level at output RDMUX exceeds a preset value. In this way, an optimum voltage swing at the RDMUX output is obtained. The response time of the AGC can be set by an external capacitor at pin 43. There is a fixed relation between the source and sink current at this pin. This results in a fixed relationship between decay and recovery time of the gain. The AGC can be switched off by connecting pin 43 to $V_{SS}$. In this condition the preamplifier gains are maximum, as specified in Chapter “Characteristics”.

### Multiplexer

A multiplexing circuit switches the nine digital channels sequentially to the output. The AUX data is switched to the output buffer during two clock periods, the eight main data channels are all sampled for one clock period. The effective sample frequency is one tenth of the clock frequency at RDCLK. Multiplexer timing is illustrated in Fig.4.

### Analog amplifiers

For Compact Cassette operation the TDA1318 has two low-noise preamplifiers, and two amplifiers for the magnetic feedback current. The analog amplifier inputs are differential, and must be AC-coupled to the MRHs. The analog inputs are internally biased by V14.

When one of the analog inputs, INL or INR, is connected to $V_{SS}$ the circuit is set to the ADR mode. In this condition the analog amplifiers are switched OFF and four DCC preamplifiers are available for amplification of the left and right analog signals.

### Feedback amplifiers

Two feedback amplifiers are available for driving a coil in the MRH, thus providing a feedback loop in order to improve the linearity of the analog audio response. In the DCC mode the feedback amplifiers can be used for biasing the MRH (for ADR = 1).

### Current and voltage sources

Separate, adjustable low-noise current sources are present for the sense currents of the DCC MRHs. The DC output voltages V14, VA14, VD14, and V33 are derived from an internal bandgap voltage reference source.

VD14 is a reference voltage for the DCC sense current sources. VA14 (referenced to $V_{SS}$) can be used to control external sense current sources. V33 (referenced to $V_{SS}$) can be used as reference voltage for an analog-to-digital converter.

### Modes of operation

The amplifiers and sense current circuits of the DCC and CC parts can be switched ON or OFF separately by the mode switch signals CS and SD. In addition, a connection of one of the analog inputs INL or INR to $V_{SS}$ is recognized as the ADR mode, thereby providing amplification of audio signals by the DCC preamplifiers. This enables the use of heads containing only DCC readers as well as heads equipped with analog and DCC readers.

The data and analog output buffers have high-output impedance in the OFF state, thus allowing the outputs of ICs to be connected in parallel.

**Table 1** Total supply current per mode.

| MODE | CS | SD | ADR | TYP. $I_{DD} + I_{CCM}$ (mA) | MAX. $I_{DD} + I_{CCM}$ (mA) |
|---|---|---|---|---|---|
| OFF | 0 | 0 | X | <0.3 | 0.3 |
| ADC reference only | 0 | 1 | X | 1.6 | 2.2 |
| CC | 1 | 0 | 0 | 18.2 | 25.0 |
| CC via DCC inputs | 1 | 0 | 1 | 26.3 | 36.5 |
| DCC (analog and digital readers) | 1 | 1 | 0 | 31.0 | 41.0 |
| DCC (digital readers only) | 1 | 1 | 1 | 39.5 | 53.0 |

**Table 2** Modes of operation.

| MODE | CONTROL SIGNAL | | | DCC PART | CC PART | FB AMPS | ADC REF | OUTPUTS SWITCHED OFF | OUTPUTS ENABLED |
|---|---|---|---|---|---|---|---|---|---|
| | CS | SD | ADR[1] | | | | | | |
| OFF | 0 | 0 | X | off | off | off | off | OUTX; RDMUX; OUTL; OUTR | – |
| ADC reference only | 0 | 1 | X | off | off | off | on | OUTX; RDMUX; OUTL; OUTR | V33 |
| CC | 1 | 0 | 0 | off | on | on | off | OUTX; RDMUX | OUTL; OUTR |
| CC via DCC inputs | 1 | 0 | 1 | on[2] | on[3] | on | off | OUTX; RDMUX | OUTL; OUTR |
| DCC (analog and digital readers) | 1 | 1 | 0 | on | off | off | on | OUTL; OUTR | V33; OUTX; RDMUX |
| DCC (digital readers only) | 1 | 1 | 1 | on | off | on | on | OUTL; OUTR | V33; OUTX; RDMUX |

**Notes**

1. ADR = 1 when pin INL and/or INR is connected to $V_{SS}$.
2. Preamplifiers only; AGC disabled.
3. Output stages only; VA14 off.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | $V_{SS}$ = 0; $V_{EEM}$ = 0 | −0.3 | 5.5 | V |
| $V_{CCM}$ | supply voltage feedback amplifiers | | −0.3 | 5.5 | V |
| $\Delta V$ | difference in ground potential between $V_{SS}$ and $V_{EEM}$ | | 0 | 0 | V |
| $V_I$ | voltage on any pin | $V_{DD}$ + 0.5 < 5.5 V | 0.3 | $V_{DD}$ + 0.5 | V |
| $I_{EEM}$ | maximum ground current (pin 28) | | – | ±120 | mA |
| $I_{CCM}$ | maximum supply current (pin 29) | | – | ±120 | mA |
| $I_n$ | maximum current on pins 24, 26, 30 and 32 | | – | ±80 | mA |
| $I_{DD}$ | maximum supply current (pin 38) | | – | ±80 | mA |
| $I_{SS}$ | maximum ground current (pin 39) | | – | ±80 | mA |
| $I_{max}$ | maximum current on all other pins | | – | ±20 | mA |
| $P_{tot}$ | total power dissipation | | – | 350 | mW |
| $T_{stg}$ | storage temperature | | −65 | +150 | °C |
| $T_{amb}$ | operating ambient temperature | | −30 | +85 | °C |
| $V_{es}$ | electrostatic handling | | −2000 | +2000 | V |

### THERMAL RESISTANCE

| SYMBOL | PARAMETER | THERMAL RESISTANCE |
|---|---|---|
| $R_{th\ j\text{-}a}$ | from junction to ambient in free air | 90 K/W |

### CHARACTERISTICS

$V_{DD}$ = 5 V; $V_{CCM}$ = 5 V; $V_{SS}$ = $V_{EEM}$ = 0 V; $f_{clk}$ = 3.072 MHz; $T_{amb}$ = 25 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $V_{DD}$ | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $V_{CCM}$ | supply voltage feedback amplifiers | | 4.5 | 5.0 | 5.5 | V |
| $I_{DDDCC}$ | supply current DCC part | CS = 1; SD = 1; ADR = 0 | 21 | 31 | 41 | mA |
| | | CS = 1; SD = 1; ADR = 1 | 21 | 31 | 41 | mA |
| $I_{DDCC}$ | supply current CC amplifiers | CS = 1; SD = 0; ADR = 0 | 7 | 9.7 | 13 | mA |
| | | CS = 1; SD = 0; ADR = 1 | 12.5 | 17.8 | 24.5 | mA |
| $I_{CCM}$ | supply current feedback amplifiers | note 1 | 6.0 | 8.5 | 12 | mA |
| $I_{DD}$ | supply current (ADC reference ON) | CS = 0; SD = 1 | 1.1 | 1.6 | 2.2 | mA |
| $I_{tot}$ | total current in OFF state of $I_{DD}$ and $I_{CCM}$ | CS = 0; SD = 0 | – | – | 300 | µA |
| $V_{ref}$ | reference voltage for DCC inputs (pin 21) | $I_o$ < –1 mA | 1.3 | 1.4 | 1.5 | V |
| | reference voltage for DCC sense (pin 7) | $I_o$ < –20 µA | 1.25 | 1.4 | 1.55 | V |
| | reference voltage for CC sense (pin 35) | $I_o$ < –20 µA | 1.25 | 1.4 | 1.6 | V |
| | reference voltage for ADC (pin 36) | $I_o$ < –2.5 mA | 3.2 | 3.3 | 3.4 | V |
| **DCC part** | | | | | | |
| AMPLIFIER CHANNEL 0 TO 7; NOTE 2 | | | | | | |
| G | amplifier gain | $f_i$ = 50 kHz | 75 | 78 | 81 | dB |
| | | $f_i$ = 100 kHz | 75 | 80 | 83 | dB |
| ΔG | relative gain | $f_i$ = 10 kHz; note 3 | –14 | –12 | –10 | dB |
| | | $f_i$ = 300 kHz; note 3 | –22 | –12 | –3 | dB |
| $V_O$ | DC output voltage | note 4 | 1.8 | 2.1 | 2.4 | V |
| $V_{os}$ | DC offset voltage between channels | note 4 | – | – | 300 | mV |
| $V_{n(ref)}$ | input referred noise voltage | $f_i$ = 50 kHz; $R_{source}$ = 70 Ω | – | 1.9 | – | nV√Hz |
| $\Delta V_{n(ref)}$ | 3 × standard deviation in amplitude spread of input referred noise | $f_i$ = 50 kHz; $R_{source}$ = 70 Ω | – | 0.5 | – | nV√Hz |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| THD | total harmonic distortion | $f_i$ = 10 kHz; $V_1$ = 0.5 V (RMS) | – | –40 | –30 | dB |
| $Z_i$ | input impedance to $V_{SS}$ | | 8 | 11 | – | kΩ |
| SR | supply rejection | $f_i$ = 50 kHz; note 5 | – | –18 | –30 | dB |
| $\alpha_{cs}$ | channel separation | $f_i$ = 10 kHz | 30 | 40 | – | dB |
| AMPLIFIER AUXILIARY CHANNEL; CHANNEL X; NOTE 2 | | | | | | |
| $G_2$ | amplifier gain at pin 2 | $f_i$ = 100 Hz to 100 kHz | 48 | 51 | 54 | dB |
| $G_1$ | amplifier gain at pin 1 | $f_i$ = 100 Hz to 100 kHz; note 6 | 62 | 65 | 68 | dB |
| $V_{n(ref)}$ | input referred noise voltage | $f_i$ = 10 kHz; $R_{source}$ = 70 Ω | – | 1.9 | – | nV√Hz |
| $\Delta V_{n(ref)}$ | 3 × standard deviation in amplitude spread of input referred noise | $f_i$ = 10 kHz; $R_{source}$ = 70 Ω | – | 0.5 | – | nV√Hz |
| $V_{2(rms)}$ | maximum output voltage (RMS value) | $f_i$ = 10 kHz | 0.5 | – | – | V |
| THD | total harmonic distortion | $f_i$ = 1 kHz; $V_1$ = 0.5 V (RMS) | – | –40 | –30 | dB |
| SR | supply rejection | $f_i$ = 1 kHz; note 5 | – | –6 | –15 | dB |
| $R_{L(DC)}$ | DC load to $V_{SS}$ (pin 2) | | 10 | – | – | kΩ |
| $C_{L(AC)}$ | AC load to $V_{SS}$ (pin 2) | | – | – | 100 | pF |
| $Z_o$ | output impedance at pin 2 in OFF state | see Table 2 | 1 | – | – | MΩ |
| OUTPUT BUFFER: PIN 1 (RDMUX) | | | | | | |
| $V_{1(rms)}$ | maximum output voltage (RMS value) | $R_L$ = 2 kΩ | 0.5 | – | – | V |
| $R_{L(DC)}$ | DC load to $V_{SS}$ | | 2 | – | – | kΩ |
| $t_{set}$ | settling time | $R_L$ = 2 kΩ; $C_L$ = 100 pF; settling within 10 mV | – | 100 | 150 | ns |
| $Z_o$ | output impedance in OFF state | see Table 1 | 1 | – | – | MΩ |
| $V_{1(rms)}$ | AGC level (RMS value) | note 7 | 120 | 270 | 410 | mV |
| $\Delta V_1$ | AGC voltage range | | 8 | 9.5 | 12 | dB |
| $I_{source}$ | AGC source current (pin 43) | | – | 80 | – | µA |
| $I_{sink}$ | AGC sink current (pin 43) | | – | 0.7 | – | µA |
| SELECTED LOGIC AND MODE SWITCH: PINS RDCLK, RDSYNC, CS AND SD | | | | | | |
| $V_{IH}$ | HIGH level input voltage | | 2.2 | – | 5.0 | V |
| $V_{IL}$ | LOW level input voltage | | 0 | – | 1.0 | V |
| $I_{LI}$ | input leakage current | | –10 | 0 | +10 | µA |
| $C_i$ | input capacitance | note 8 | – | – | 10 | pF |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $t_{su}$ | set-up time RDCLK and RDSYNC | note 9 | 20 | – | – | ns |
| $t_h$ | hold time RDCLK and RDSYNC | note 9 | 20 | – | – | ns |
| $t_r$ | rise time | note 9 | – | – | 50 | ns |
| $V_{ADR}$ | ADR mode detection level (pins 25 and 31) | | 0 | – | 0.4 | V |
| $V_{TEST}$ | test mode detection level (pin 27) | | 0 | – | 0.4 | V |
| SENSE CURRENT SOURCE | | | | | | |
| $I_{DSEN(min)}$ | minimum output current | note 10 | – | – | 5 | mA |
| $I_{DSEN(max)}$ | maximum output current | note 11 | 20 | – | – | mA |
| $I_{no}$ | output noise current | note 11 | – | 20 | – | pA√Hz |
| $Z_o$ | output impedance | $I_{DSEN}$ = 10 mA | 20 | – | – | kΩ |
| **CC part** | | | | | | |
| ANALOG AMPLIFIER | | | | | | |
| G | amplifier gain | $f_i$ = 20 Hz to 20 kHz | 43 | 45 | 47 | dB |
| $V_{i(rms)}$ | input voltage level (RMS value) | $f_i$ = 1 kHz | – | 2.75 | – | mV |
| $V_{n(ref)}$ | input referred noise voltage | $f_i$ = 10 kHz; $R_{source}$ = 300 Ω | – | 2.8 | – | nV√Hz |
| $\Delta V_{n(ref)}$ | 3 × standard deviation in amplitude spread of input referred noise | $f_i$ = 10 kHz; $R_{source}$ = 300 Ω | – | 1.0 | – | nV√Hz |
| $V_{o(rms)}$ | maximum output voltage (RMS value) | $f_i$ = 1 kHz | 0.5 | – | – | V |
| THD | total harmonic distortion | $f_i$ = 1 kHz; $V_o$ = 0.5 V (RMS) | – | –60 | –50 | dB |
| SR | supply rejection | $f_i$ = 1 kHz; note 5 | – | 37 | – | dB |
| $\alpha_{cs}$ | channel separation | $f_i$ = 1 kHz | 40 | – | – | dB |
| $R_{L(DC)}$ | DC load to $V_{SS}$ (pins 22 and 34) | | 10 | – | – | kΩ |
| $C_{L(AC)}$ | AC load to $V_{SS}$ (pins 22 and 34) | | – | – | 300 | pF |
| $Z_o$ | output impedance in OFF state (pins 22 and 34) | see Table 2 | 1 | – | – | MΩ |
| ANALOG INPUT VIA DCC PREAMPLIFIERS | | | | | | |
| G | amplifier gain | $f_i$ = 20 Hz to 20 kHz | 48 | 51 | 54 | dB |
| $V_{i(rms)}$ | input voltage level (RMS value) | $f_i$ = 1 kHz | – | 1.4 | – | mV |
| $V_{n(ref)}$ | input referred noise voltage | $f_i$ = 10 kHz; $R_{source}$ = 70 Ω | – | 1.9 | – | nV√Hz |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $\Delta V_{n(ref)}$ | 3 × standard deviation in amplitude spread of input referred noise | $f_i$ = 10 kHz; $R_{source}$ = 70 Ω | – | 0.5 | – | nV√Hz |
| $V_{o(rms)}$ | maximum output voltage (RMS value) | $f_i$ = 1 kHz | 0.5 | – | – | V |
| THD | total harmonic distortion | $f_i$ = 1 kHz; $V_1$ = 0.5 V (RMS) | – | –40 | –30 | dB |
| SR | supply rejection | $f_i$ = 1 kHz; auxiliary data channel; see Fig.6 | – | –6 | – | dB |
| $\alpha_{cs}$ | channel separation | $f_i$ = 1 kHz | 40 | – | – | dB |
| FEEDBACK AMPLIFIER | | | | | | |
| $I_{o(rms)}$ | maximum output current (RMS value) | note 12 | 30 | – | – | mA |
| THD | total harmonic distortion | note 13 | – | –60 | –50 | dB |
| B | bandwidth | note 14 | 50 | – | – | kHz |

**Notes**

1. CS = 1, SD = 1, ADR = 1; CS = 1, SD = 0, ADR = 0; CS = 1, SD = 0, ADR = 1; feedback amplifiers unloaded. The supply pins for the feedback amplifiers are pins 28 and 29. The supply pins for all other circuits are pins 38 and 39 (see Tables 1 and 2).
2. AGC circuit OFF (maximum gain; pin 43 connected to $V_{SS}$).
3. Gain relative to gain at $f_i$ = 50 kHz. See Fig.5 for typical frequency response.
4. Difference between minimum and maximum DC level at the outputs of the data channels. To be measured at pin 1.
5. See Figs 6 and 7 for typical supply rejection.
6. Pin 2 AC-coupled to pin 3 via 100 nF capacitor.
7. Measured with a continuous sinewave of 10 kHz at pin 1, multiplexer in a fixed position. A 1 V (RMS) sinewave corresponds with a multiplexed DCC signal of 4.3 V (p-p).
8. Periodically sampled, not tested.
9. Timing relationship between the edges of RDCLK and RDSYNC is illustrated in Fig.3. Figure 4 illustrates the action of the multiplexer switches.
10. The output current can be adjusted by connecting a resistor between the adjust pin and $V_{SS}$. A 68 Ω resistor will produce 10 mA (typ.) through the MRHs (see Fig.9).
11. A resistor of 210 Ω connected between sense current output and $V_{DD}$; frequency range from 10 kHz to 100 kHz; sense current = 10 mA; pin 7 decoupled to $V_{SS}$ by 10 μF capacitor.
12. Closed loop; unity gain; $f_i$ = 1 kHz; THD < –45 dB; $R_L$ = 40 Ω; in accordance with Fig.10.
13. Closed loop; unity gain; $f_i$ = 1 kHz; 10 mA (RMS) output current into 40 Ω; in accordance with Fig.10.
14. Closed loop; unity gain; –3 dB bandwidth; measured in test circuit of Fig.10.

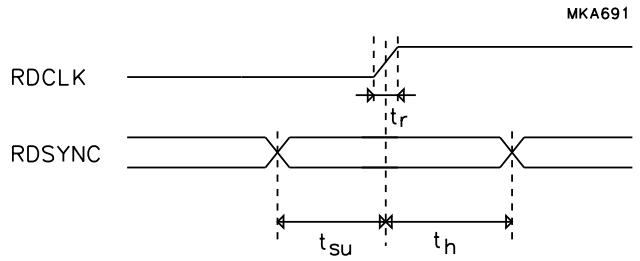



Fig.3 Timing relationship between the edges of RDCLK and RDSYNC.

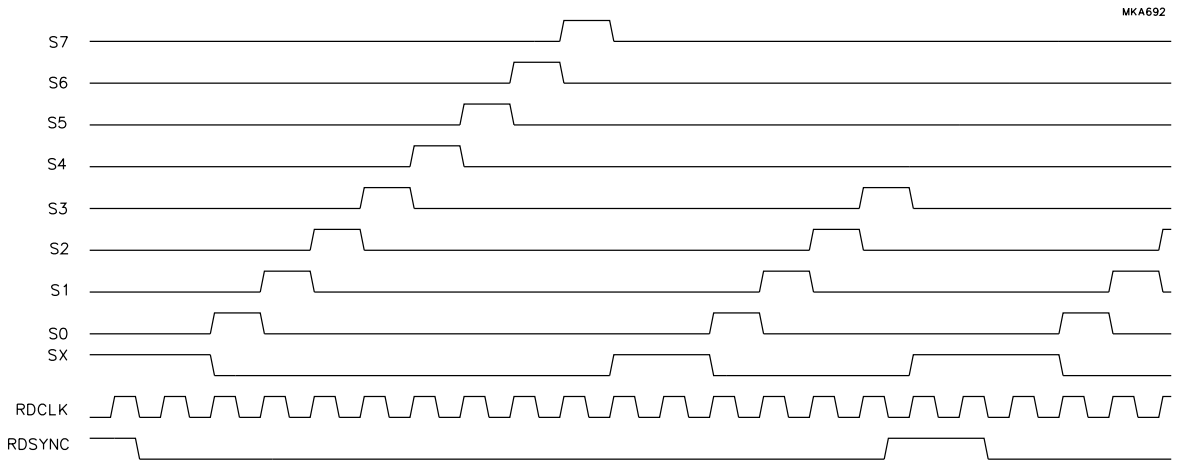



Fig.4 Multiplexer timing diagram.

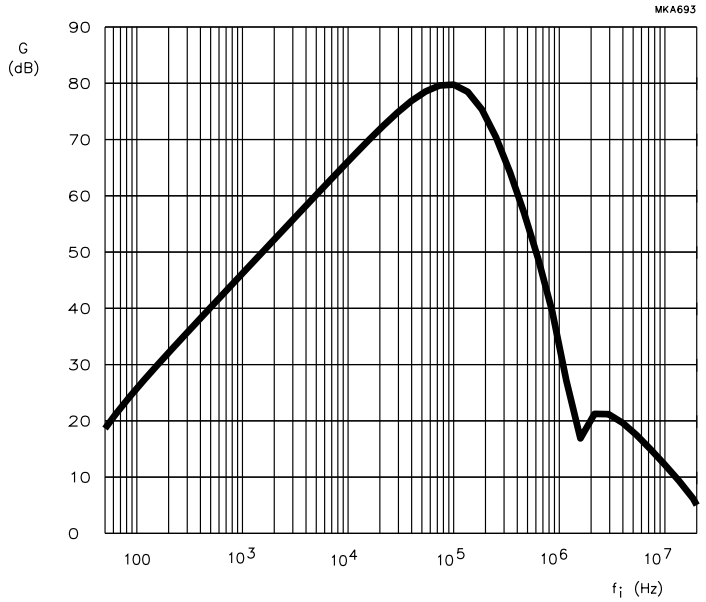



Fig.5 Typical gain of main data channel (AGC off).

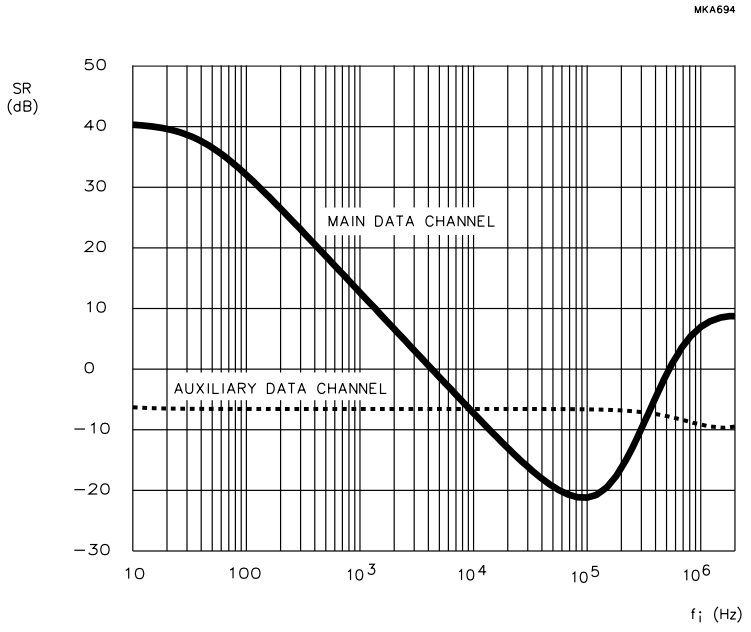



Fig.6 Typical supply rejection of main data and auxiliary data channel (AGC off).

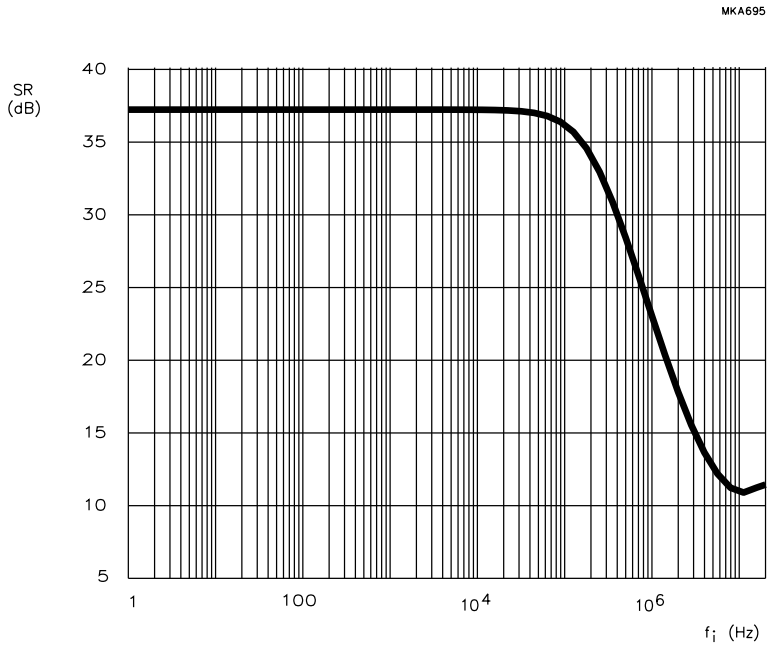



Fig.7 Typical supply rejection of analog amplifier.

**TEST INFORMATION**

The circuit can be set to the TEST mode by connecting pin 27 to $V_{SS}$. In this configuration the multiplexer at pin 3 allows monitoring of the input stage and low-pass filter of each digital amplifier, and also allows input to the high-pass filter of the second stage. The test multiplexer operates in phase with the output multiplexer.

Measurement of the gain of the digital channels can be carried out in two steps: the gain from DCC input to pin 3, and the gain from pin 3 to pin 1.

Figure 8 illustrates how to use pin 3 in the test mode; $C_L$ < 20 pF, $R_L$ > 100 kΩ, $C_i$ > 47 nF, $R_{bias}$ = 1 kΩ. The DC voltage, when driving pin 3, should be 0.7 V greater than the measured DC level at pin 3 in order to shut-off the emitter follower. The impedance of the sense current source outputs can be measured from the difference in sense current when applying different voltages to the sense current output. This voltage can vary from 1.5 V to $V_{DD}$. Figure 9 illustrates the principle of the sense current sources.

The feedback amplifiers consist of two operational amplifiers providing one input and a differential output with respect to the internal 2.5 V reference (see Fig.10).

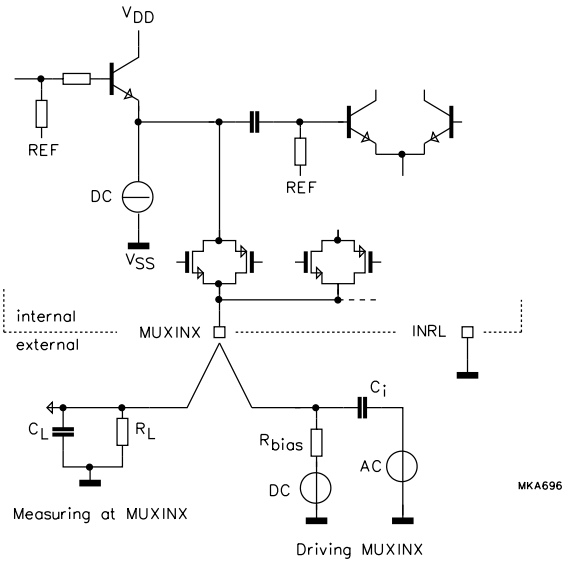



Fig.8 Test by using MUXINX (pin 3).

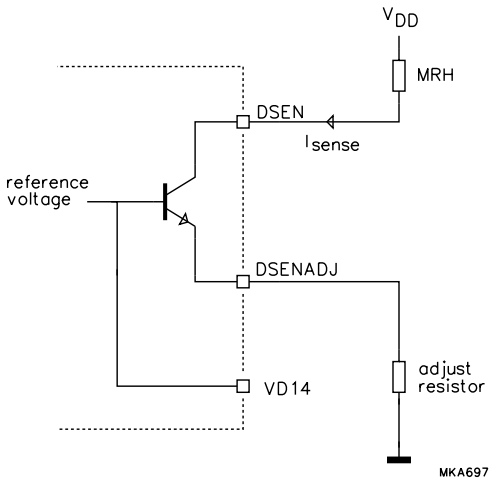



Fig.9 Principle of the sense current source.

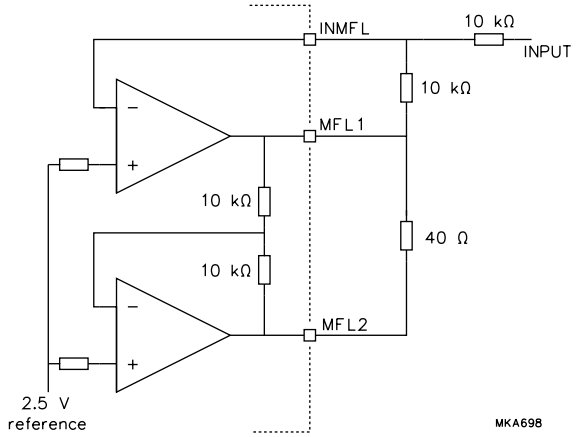



Fig.10 Principle of the feedback amplifier and test circuit.

**APPLICATION INFORMATION**

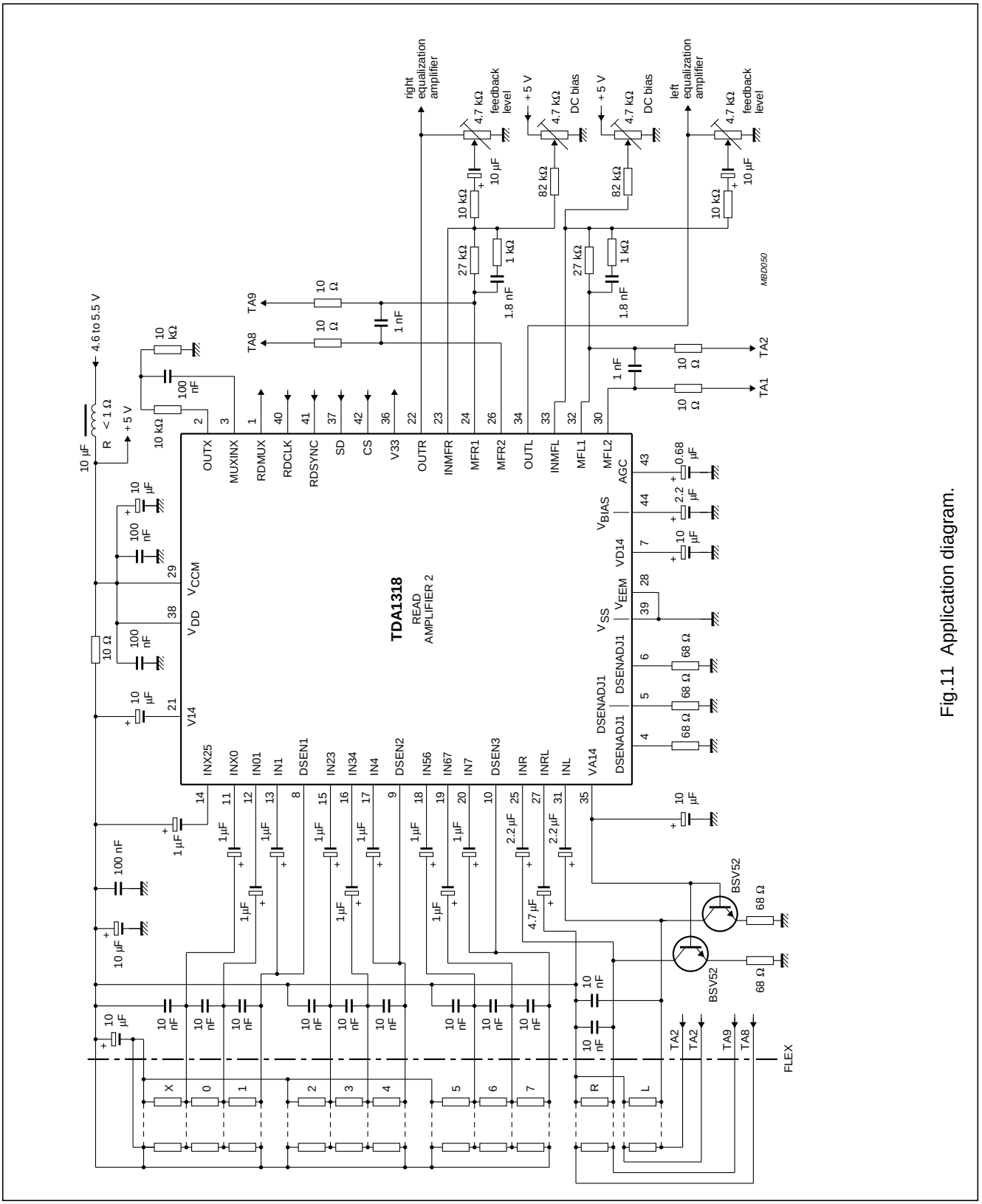



Fig.11 Application diagram.

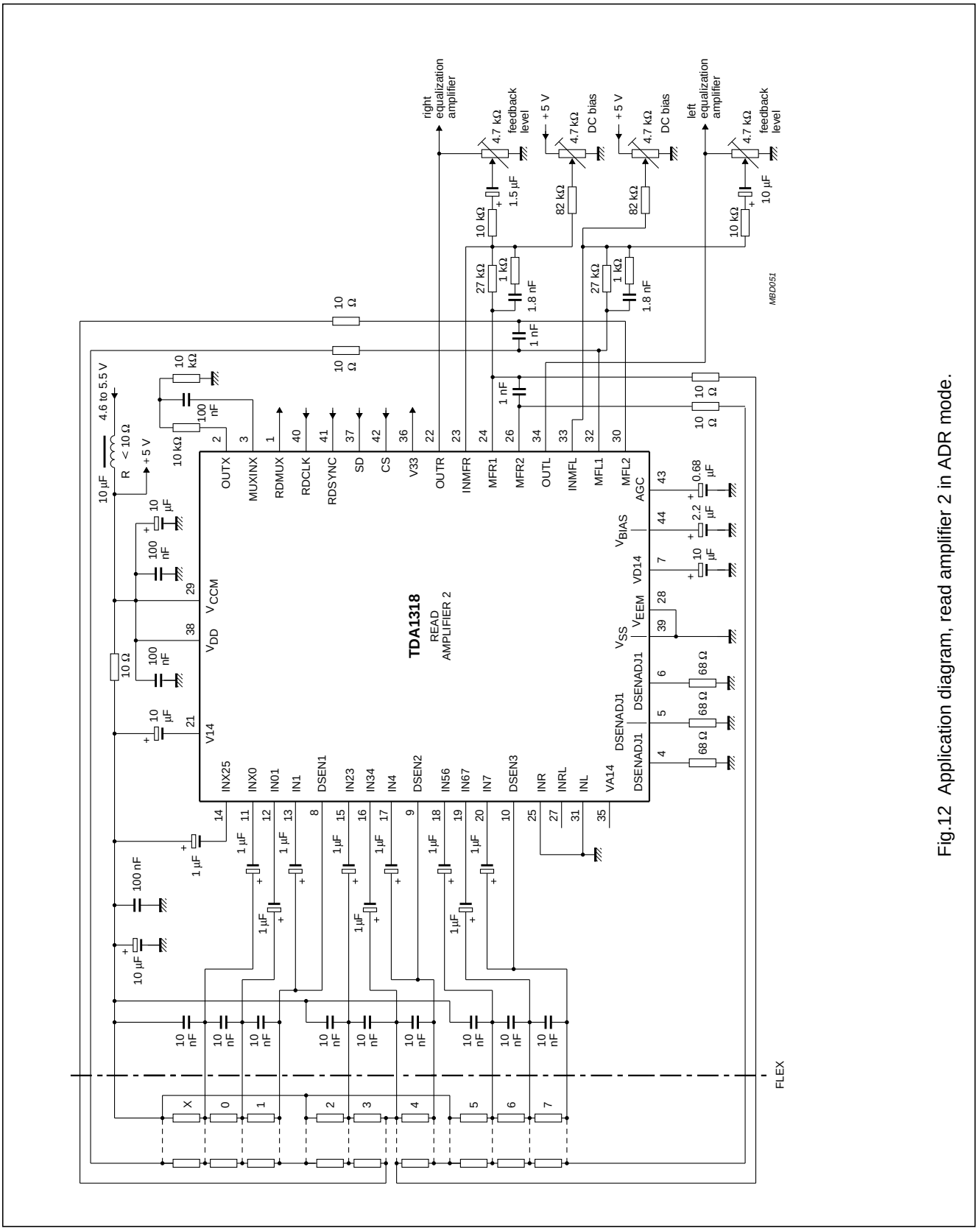



Fig.12 Application diagram, read amplifier 2 in ADR mode.

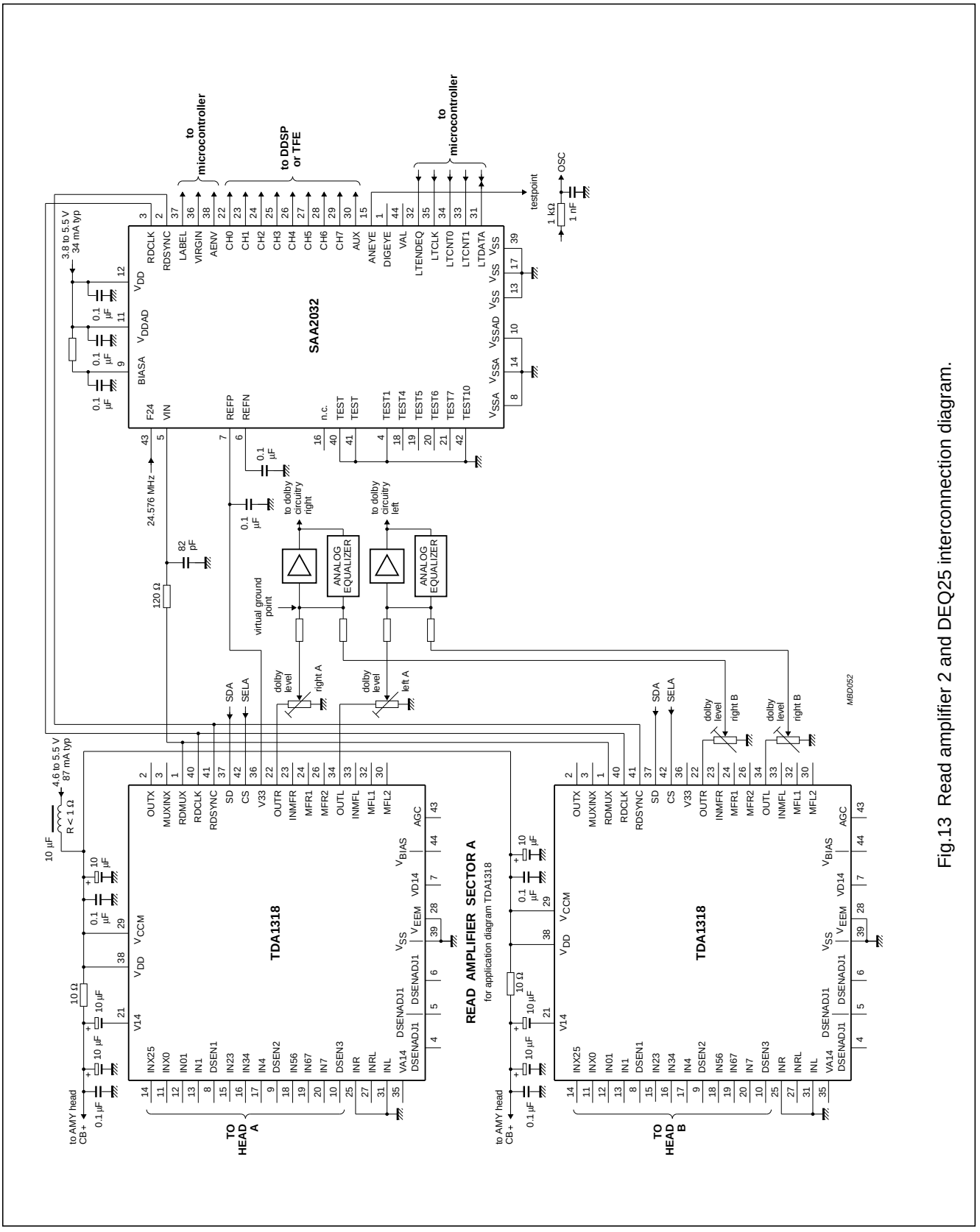
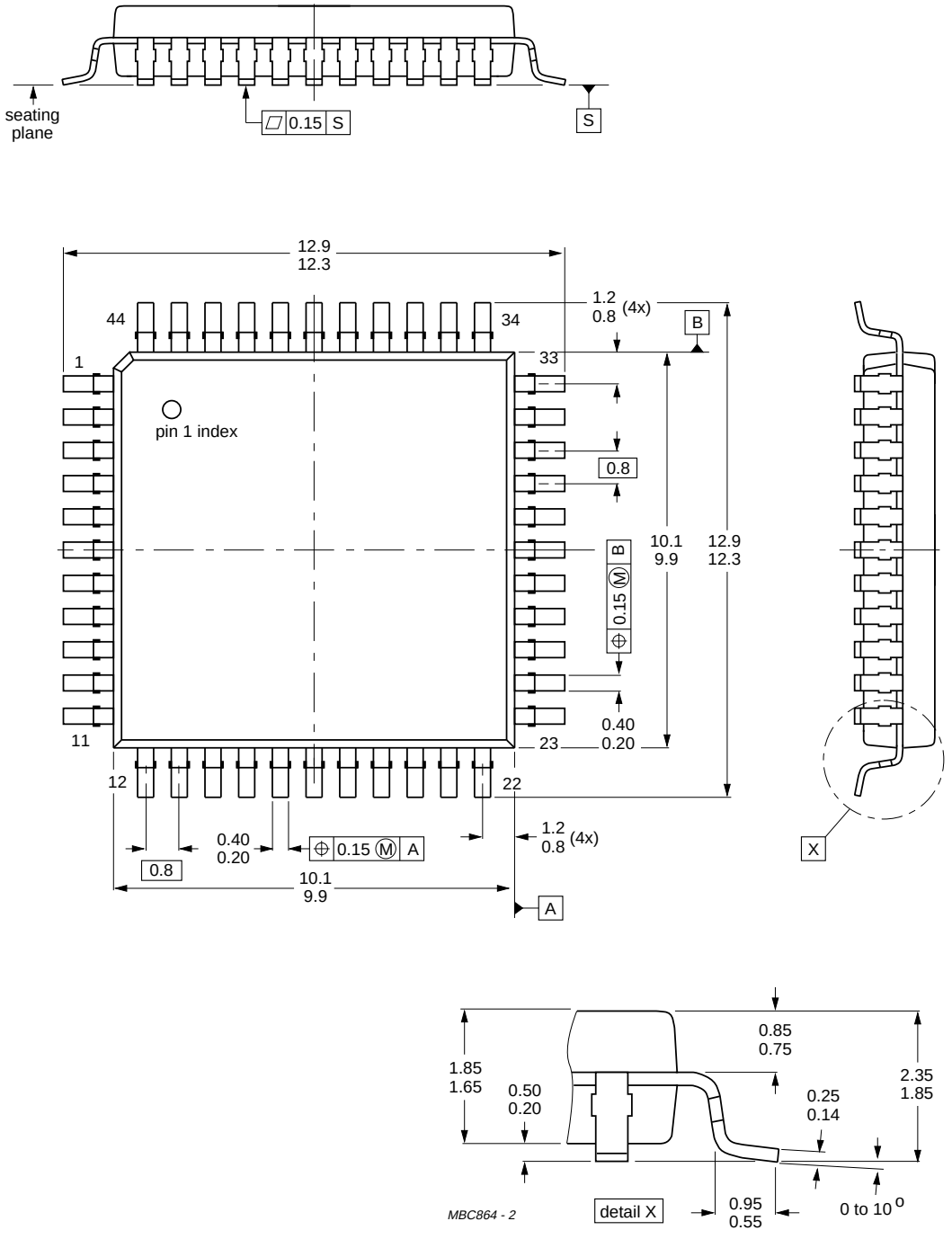



Fig.13 Read amplifier 2 and DEQ25 interconnection diagram.

**PACKAGE OUTLINE**




Dimensions in mm.

Fig.14 44-lead quad flat-pack; plastic (QFP44S10, SOT307-2).

## SOLDERING

### Plastic quad flat-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

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| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
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