Integrated VIP and teletext decoder (IVT2.0)

SAA5260

FEATURES

- Complete teletext decoder in a single 48-pin DIL package
- Single +5 V power supply
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Both video and scan related synchronization modes are supported
- 4096 colour palette, with 16 different foreground plus 16 different background colours
- Full row and border background colours covering the whole screen area
- Background colour control characters for highlighting text areas
- 224 characters in ROM (12 x 10 matrix), giving wide language coverage and additional graphics symbols for on-screen displays
- Double width and double size decoding as well as double height
- Foreground character processing for language extension possible without display flicker
- Analog RGB outputs with simple interface to colour decoder ICs
- Data capture performance similar to SAA5231 (VIP2)
- 5 channel acquisition system for fast page capture
- Pointer system to connect any acquisition channel to any page memory
- Interfaces to 32 K x 8-bit static RAM (8 K x 8 also possible)
- Extension packet option including full error correction in hardware (8/4 and 24/18 Hamming)
- 7-bit + parity, 8-bit, full page Hamming and mixed Hamming/7-bit + parity acquisition options, selected per channel to allow e.g. optimum TOP decoding
- End of page detectors with interrupt generation for fast data processing
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I²C-bus
- Automatic ODD/$\overline{\text{EVEN}}$ output control with manual override
- Control of display PLL free-run and rolling header via I²C-bus
- VCS to SCS mode for stable 525 line status display
- Option for battery back-up of page memory.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5	5.5	V
I_{DD}	supply current	–	75	150	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature range	−20	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5260P/E	48	DIL	plastic	SOT240

DESCRIPTION

The SAA5260 is a single-chip teletext decoder IC for decoding 625-line based World System Teletext transmissions. The device is based on the IVT1.0 (SAA5246) with additional features to provide a higher performance decoder. A larger memory (32 K x 8) can be connected for faster access to pages and better display facilities are provided, including more symbols and colours.

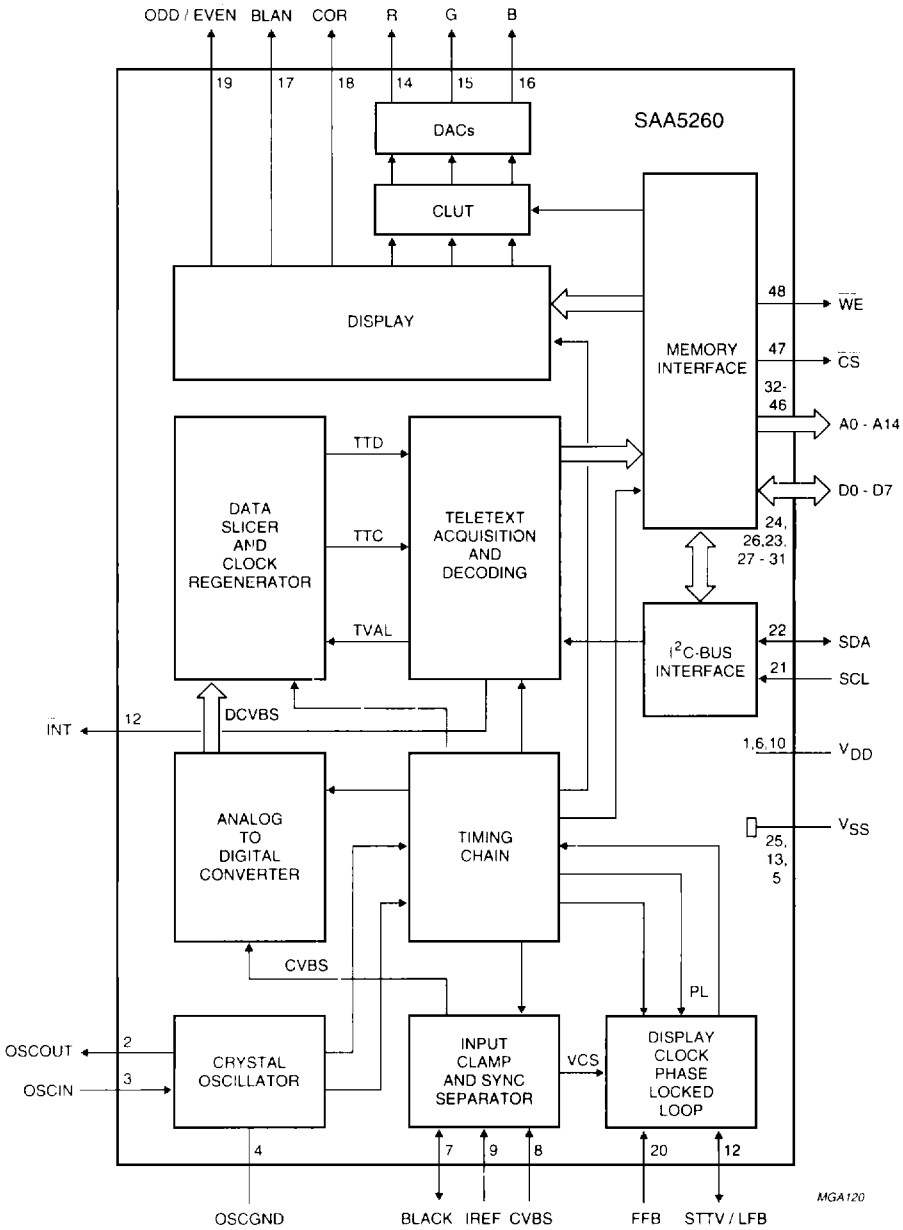


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD}	1, 6, 10	+5 V supply
OSCOUT	2	27 MHz crystal oscillator output
OSCIN	3	27 MHz crystal oscillator input
OSCGND	4	0 V crystal oscillator ground
V_{SS}	5, 13, 25	0 V ground
BLACK	7	video black level storage pin, connected to ground via a 100 nF capacitor
CVBS	8	composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	9	reference current input pin, connected to ground via a 27 kΩ resistor
STTV/LFB	11	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{INT}$	12	interrupt output from end of page detector, X/27, X/29 and 8/30 flags
R	14	dot rate character output of the RED colour information
G	15	dot rate character output of the GREEN colour information
B	16	dot rate character output of the BLUE colour information
BLAN	17	dot rate fast blanking output
$\overline{COR}$	18	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open drain output
ODD/$\overline{EVEN}$	19	25 Hz output synchronized with the CVBS input's field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents
FFB	20	field flyback input
SCL	21	serial clock input for I²C-bus. It can still be driven HIGH during power-down of the device
SDA	22	serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during power-down of the device
D2	23	data input/output for external RAM
D0	24	data input/output for external RAM
D1	26	data input/output for external RAM
D3 to D7	27 to 31	data inputs/outputs for external RAM
A0 to A14	32 to 46	address outputs for external RAM
$\overline{CS}$	47	output to RAM if memory not to be cleared on power-up
$\overline{WE}$	48	write enable to external RAM

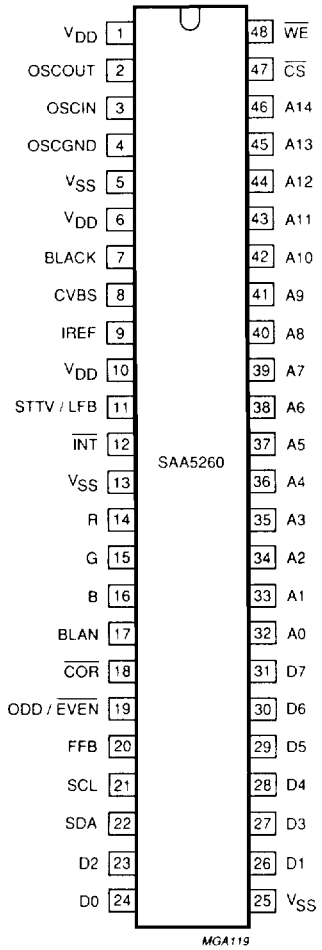


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	6.5	V
V_I	input voltage (any input)	−0.3	V_{DD}+0.5	V
V_O	output voltage (any output)	−0.3	V_{DD}+0.5	V
I_O	output current (each output)	−	±10	mA
I_{IOK}	DC input or output diode current	−	±20	mA
T_{amb}	operating ambient temperature range	−20	70	°C
T_{stg}	storage temperature range	−55	125	°C
V_{stat}	electrostatic handling human body model (note 1)	−2000	2000	V

Note

1. The human body model ESD simulation is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor; this produces a single discharge transient. Reference Philips Semiconductors test method UZW-B0/FQ-A302 (compatible with MIL-STD method 3015.7).

Failure Rate

The failure rate at T_{amb} = 55 °C will be a maximum of 1000 FITS (1 FIT = 1 x 10^{-9} failures per hour).

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −20 to +70 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		4.5	5	5.5	V
I_{DD}	total supply current		–	75	150	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
t_{syn}	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		−150	0	150	ns
t_{syd}	change in CVBS to TCS delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak)		0.7	1	1.4	V
	display PLL catching range		±7	–	–	%
Z_{src}	source impedance		–	–	250	Ω
C_I	input capacitance		–	–	10	pF
IREF						
R_g	resistor to ground		–	27	–	kΩ
V_g	voltage on pin 9		–	$V_{DD}/2$	–	V
LFB						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
I_I	input current	note 1	−1	–	1	mA
t_{LFB}	delay between LFB front edge and input video line sync		–	250	–	ns
FFB						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
I_I	input current	note 1	−1	–	1	mA
SCL						
V_{IL}	LOW level input voltage		−0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
f_{SCL}	clock frequency		0	–	150	kHz
t_r	input rise time	10% to 90%	–	–	2	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_f	input fall time	90% to 10%	–	–	2	µs
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
D0 TO D7						
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
C_L	load capacitance		–	–	120	pF
SDA						
V_{IL}	LOW level input voltage		–0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
A0 TO A14 ADDRESS OUTPUT TO MEMORY						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_I	input capacitance		–	–	120	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{WE}$						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
CS						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
C_L	load capacitance		–	–	120	pF
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
R, G AND B						
R_L	load resistance to V_{SS}		–	150	–	Ω
I_{OL}	output current (black level)		−10	0	10	μA
I_{OL}	output current (full amplitude)	at nominal V_{DD}	−6.0	−6.67	−7.3	mA
C_L	load capacitance		–	–	20	pF
t_r	output rise time	10% to 90%; R_L = 150 Ω; C_L = 20 pF	–	–	20	ns
t_f	output fall time	90% to 10%; R_L = 150 Ω; C_L = 20 pF	–	–	20	ns
BLAN						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	1.1	–	–	V
V_{OH}	HIGH level output voltage	I_{OH} = 0 mA	–	–	2.8	V
V_{OH}	allowed voltage at pin	with extenal pull-up	–	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
ODD/$\overline{EVEN}$						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −1.6 mA	V_{DD}−0.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{COR}$ (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.4	V
V_{OL}	LOW level output voltage	I_{OL} = 5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} −0.5 and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	−10	–	10	μA
TSK	skew delay between display outputs R, G, B, $\overline{COR}$, and BLAN		–	–	20	ns
$\overline{INT}$ (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
I_{LO}	output leakage current		−10	–	10	μA
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 3.3 kΩ to V_{DD} measured between 4 V and 1 V	–	–	50	ns
Timing						
I²C-BUS						
f_{DAT}	I²C data rate for:					
	all registers		–	–	150	kHz
	all registers except display RAM write/reads		–	–	350	kHz
	other devices on bus (IVT will not lock up)		–	–	400	kHz
t_{LOW}	clock LOW period		1.4	–	–	μs
t_{HIGH}	clock HIGH period		1.4	–	–	μs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	μs
t_{BUF}	START set-up time following a STOP		4	–	–	μs
$t_{HD;STA}$	START hold time		1.4	–	–	μs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		1.4	–	–	μs
RAM INTERFACE						
t_{CY}	cycle time		–	500	–	ns
t_{ADDR}	address active time		450	500	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{ACC}	access time from address		–	–	150	ns
t_{DH}	data hold time from address		0	–	–	ns
t_{WE}	$\overline{WE}$ LOW from address change		40	–	–	ns
t_{WEW}	$\overline{WE}$ pulse width		100	–	–	ns
t_{DS}	data set-up time to $\overline{WE}$ HIGH		60	–	–	ns
t_{DHWE}	data hold time from $\overline{WE}$ HIGH		0	–	20	ns
t_{WR}	write recovery time		20	–	–	ns
t_{DE}	data enable from $\overline{WE}$ LOW		10	–	–	ns

Note to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

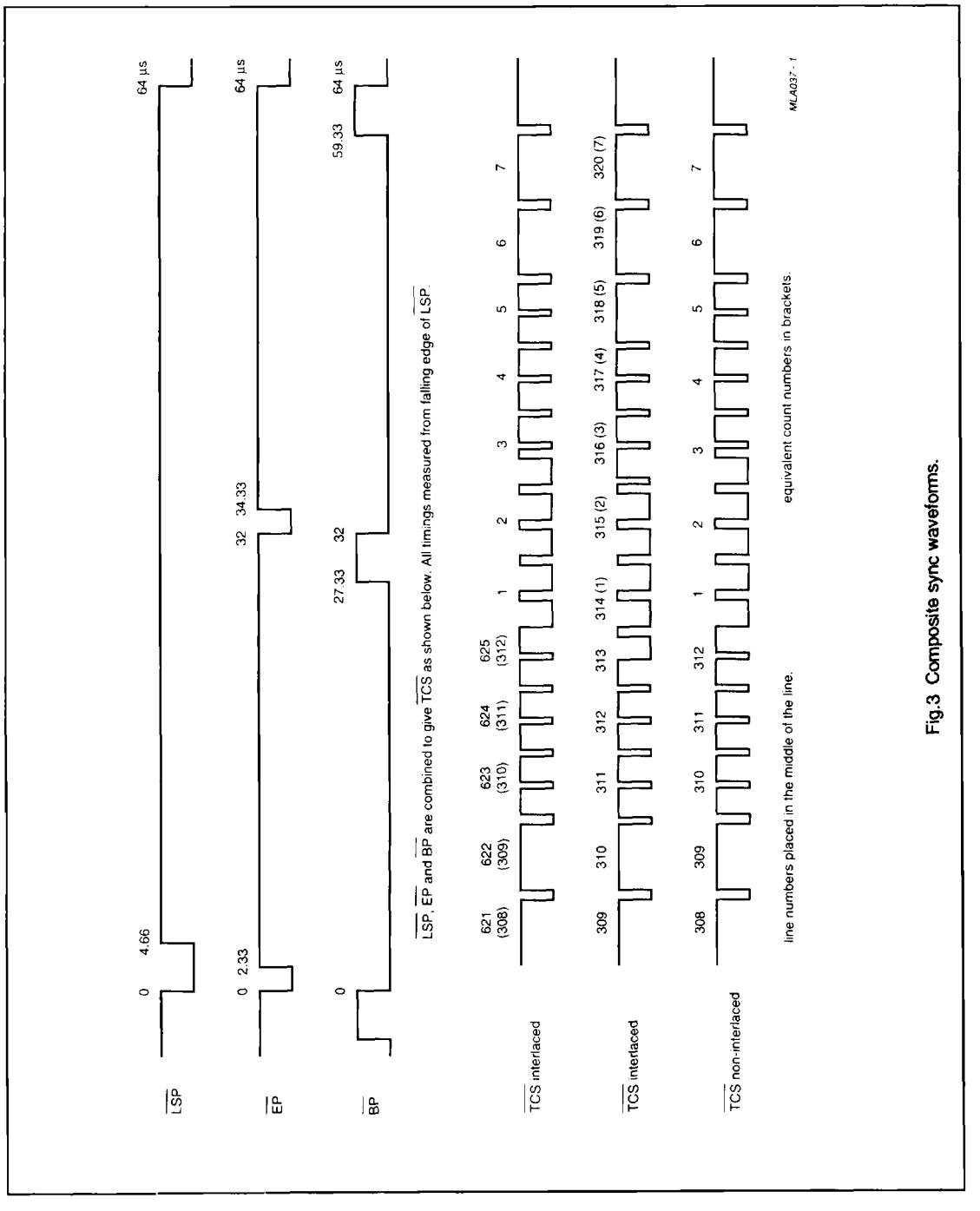


Fig.3 Composite sync waveforms.

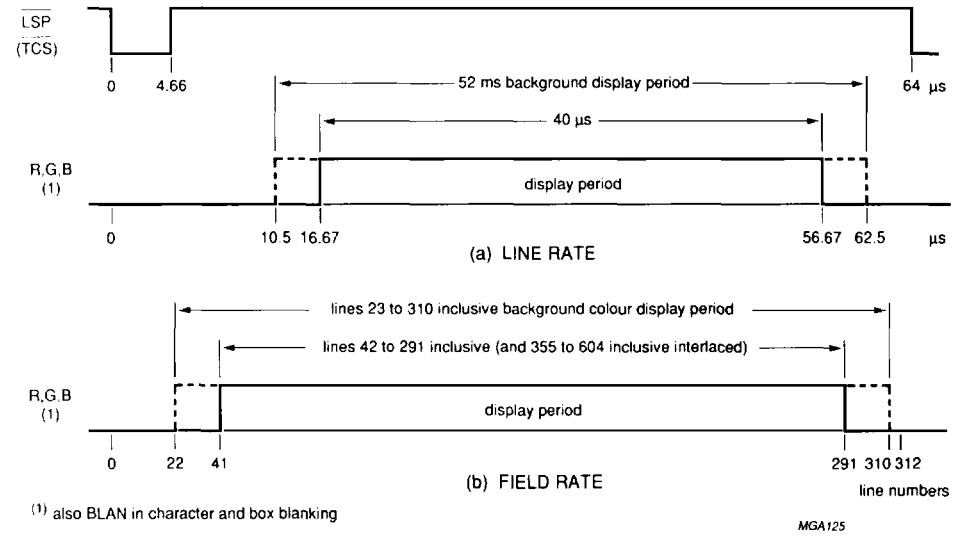


Fig.4 Display output timing (a) line rate (b) field rate.

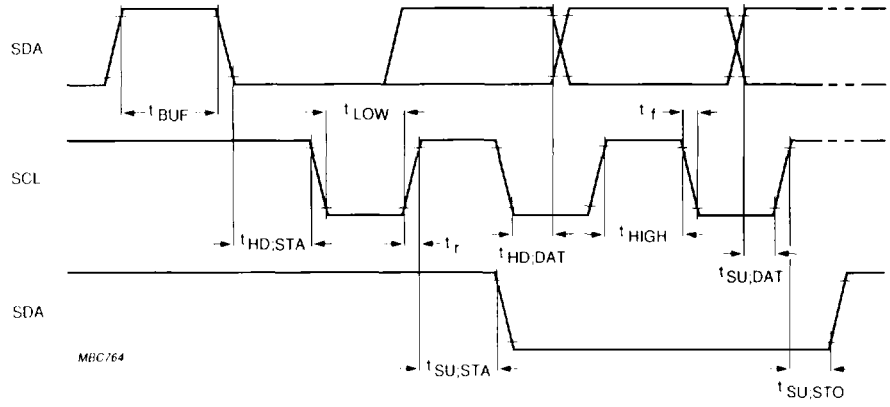


Fig.5 I²C-bus timing.

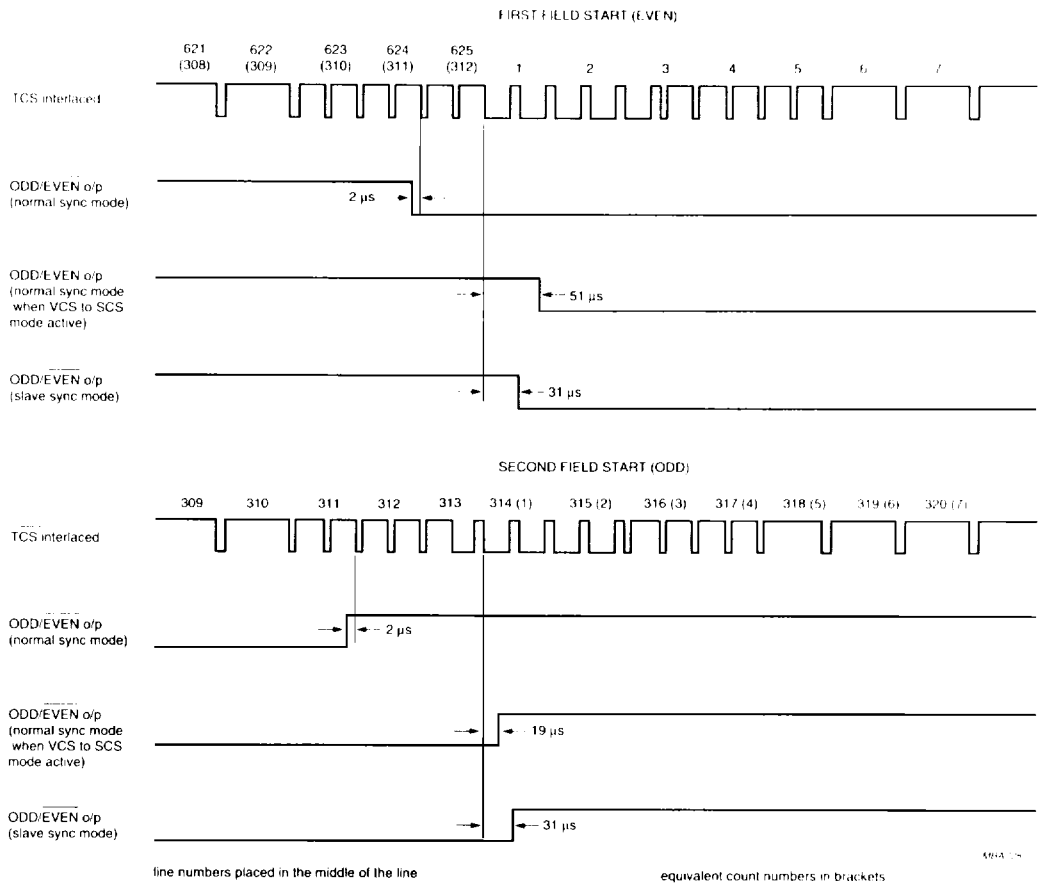


Fig.6 ODD/$\overline{\text{EVEN}}$ timing.

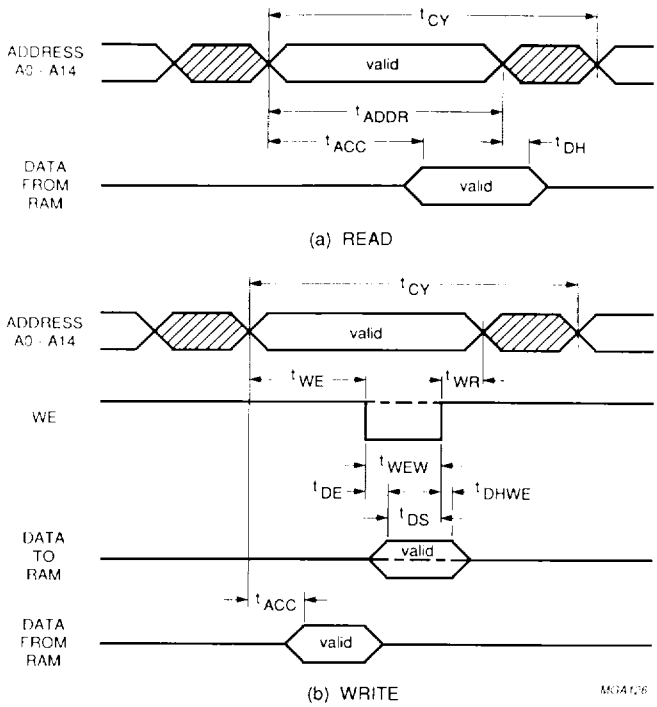


Fig.7 Memory interface timing (a) read (b) write.

APPLICATION INFORMATION

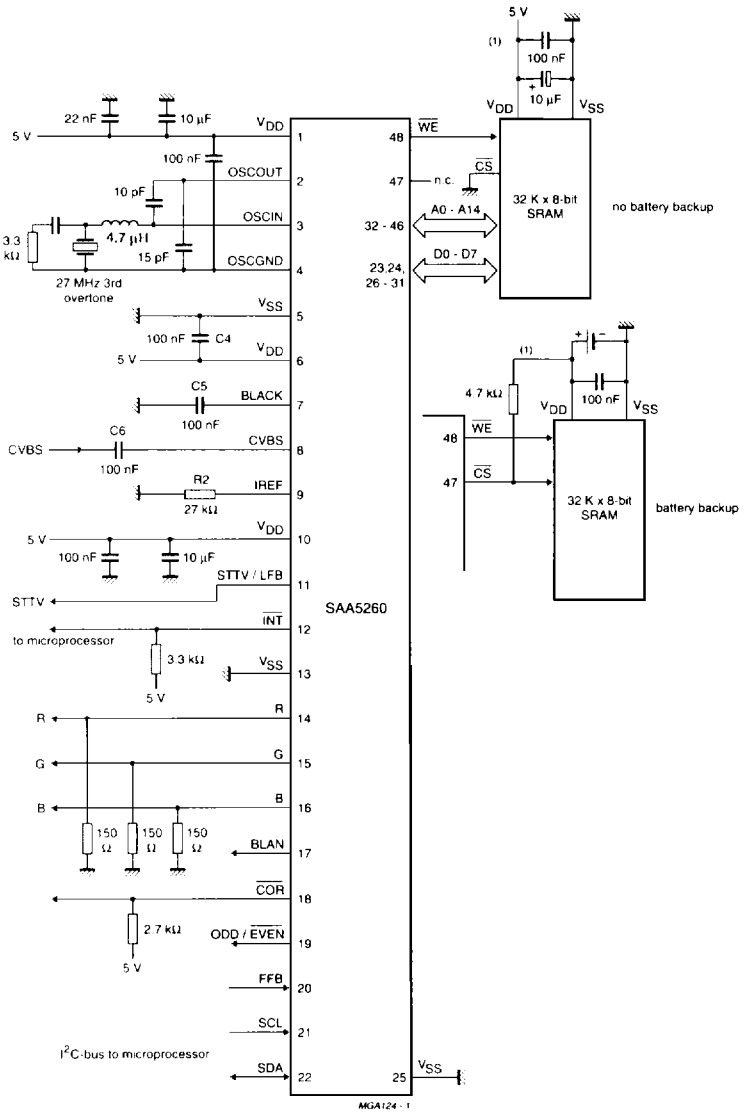
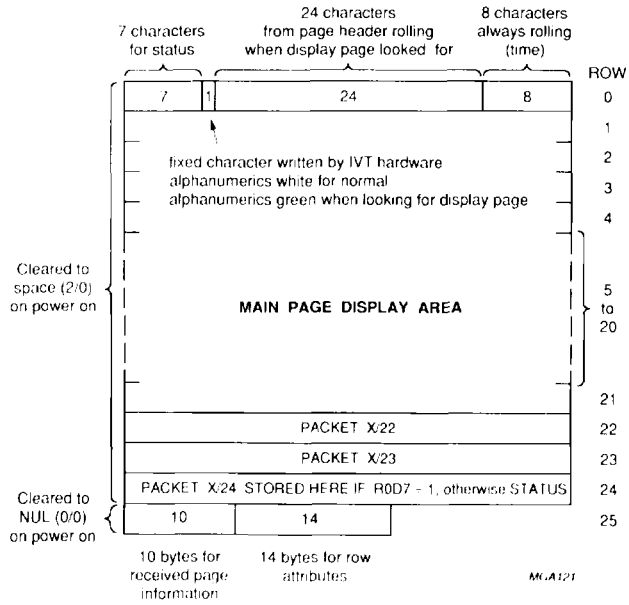


Fig.8 Application diagram.

(1) Optional connections if battery backed up memory required. The 5 V supply shown comes from battery. If battery back-up is not used, then $\overline{CS}$ of RAM is connected to ground and the $\overline{CS}$ output from the device is not used.

SAA5260 page memory organization

The organization of the page memory is shown in Fig.9. The display format is 40 characters by 25 rows. Rows 0 to 23 form the teletext page; row 24 is available for software generated status messages and FLOF/FASTEXT prompt information.



Row 0:
Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by SAA5260 to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25:
The first 10 bytes of row 25 contain control data relating to the received page as shown in Table 1.

Fig.9 Basic page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

Page number

MAG magazine

PU page units

PT page tens

PBLF page being looked for

$\overline{\text{FOUND}}$ LOW for page has been found

HAM.ER Hamming error in corresponding byte

Page sub-code

MU minutes units

MT minutes tens

HU hours units

HT hours tens

C4-C14 transmitted control bits.

The remaining 14 bytes of row 25 contain the row attributes for defining the default background colour of each row and the chapter from which it is to be displayed, as shown in Table 2.

Table 2 Row 25 row attributes

D0	TR	R0R	R2R	R4R	R6R	R8R	R10R	R12R	R14R	R16R	R18R	R20R	R22R	R24R
D1	TG	R0G	R2G	R4G	R6G	R8G	R10G	R12G	R14G	R16G	R18G	R20G	R22G	R24G
D2	TB	R0B	R2B	R4B	R6B	R8B	R10B	R12B	R14B	R16B	R18B	R20B	R22B	R24B
D3	-	DR0	DR2	DR4	DR6	DR8	DR10	DR12	DR14	DR16	DR18	DR20	DR22	DR24
D4	BR	R1R	R3R	R5R	R7R	R9R	R11R	R13R	R15R	R17R	R19R	R21R	R23R	-
D5	BG	R1G	R3G	R5G	R7G	R9G	R11G	R13G	R15G	R17G	R19G	R21G	R23G	-
D6	BB	R1B	R3B	R5B	R7B	R9B	R11B	R13B	R15B	R17B	R19B	R21B	R23B	-
D7	-	DR1	DR3	DR5	DR7	DR9	DR11	DR13	DR15	DR17	DR19	DR21	DR23	-
COLUMN	10	11	12	13	14	15	16	17	18	19	20	21	22	23

R, G and B are the settings of the default background colour attribute. They only correspond to RED, GREEN and BLUE colour outputs when the colour look-up table is in the default condition; at other times, they are simply entries in the colour look-up table.

T Top border of screen, above row 0 (or above status row if R1D7 = 1)

B Bottom border of screen, below the status row (or below row 23 if R10D7 = 1)

R1 etc. Row 1 display

DR2 etc. Display row 2 etc. defines whether the text for this display row comes from the normal display chapter register (0) or supplementary display chapter register (1)

These letters are combined as appropriate, e.g. R8R = red default background for row 8, BG = green default background for bottom screen border.

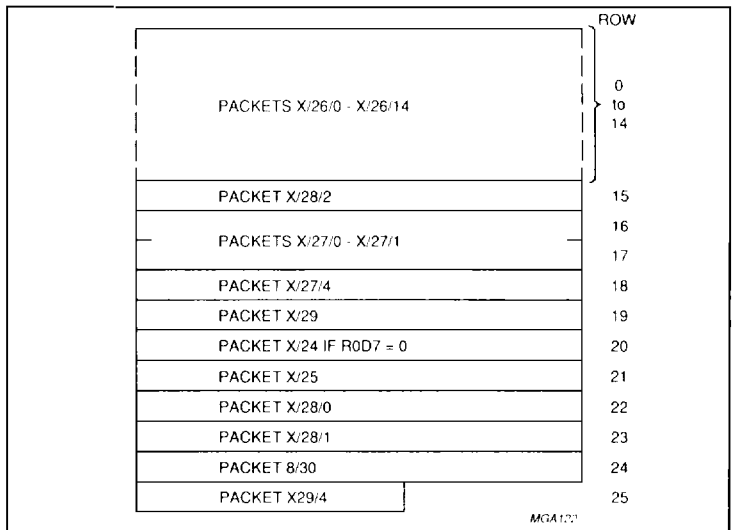


Fig.10 Organization of the extension memory.

Extension packet memory organization

When in extension packet enable mode, the rows of information are organized as shown in Fig.10.

The page-related extension packets are stored in the next higher memory chapter relative to the corresponding basic page data, e.g. basic page chapter 6, extension packets chapter 7.

Some extension packets are not page related; these are stored in the chapters as shown in Tables 3 and 4.

Packet 8/30: Stored in a chapter according to the designation code. Pairs of designation codes are stored in the same chapter, owing to the use of the LSB as a flag indicating VBI or full channel.

Table 3 Packet 8/30 storage

PACKET	CHAPTER
8/30/0, 8/30/1	1
8/30/2, 8/30/3	3
8/30/4, 8/30/5	5
8/30/6, 8/30/7	7
8/30/8, 8/30/9	9
8/30/10, 8/30/11	11
8/30/12, 8/30/13	13
8/30/14, 8/30/15	15

Packet 29: Two versions are stored in row 19, X/29/0 (for colour definition) and X/29/1 (for character set definition) and one in row 25, X/29/4.

Table 4 Packet 29 storage

PACKET	CHAPTER
8/30/0 and 4	1
1/29/0 and 4	3
2/29/0 and 4	5
3/29/0 and 4	7
4/29/0 and 4	9
5/29/0 and 4	11
6/29/0 and 4	13
7/29/0 and 4	15
8/29/1	17
1/29/1	19
2/29/1	21
3/29/1	23
4/29/1	25
5/29/1	27
6/29/1	29
7/29/1	31

Register maps

SAA5260 mode registers are shown in Table 5. R0 to R15 are WRITE only; R16A is READ/WRITE; R16B and R16C are READ only.

Table 5 Register map

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Mode	0	X24 POS	EXTN. PACKET ENABLE	$\overline{\text{DEW}}$/ FULL FIELD	DISABLE HDR ROLL	B.T. NUMBER ENABLE	POL	BOX TIME	BOX HEADER
Sync	1	VCS TO SCS	FREE RUN PLL	AUTO ODD/ $\overline{\text{EVEN}}$	DISABLE ODD/ $\overline{\text{EVEN}}$	VCR	TCS ON	T1	T0
Acq. control	2	ACQ. $\overline{\text{ON}}$/OFF	ACQ. CCT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Acq. Mode A	4	–	–	–	H4	H3	H2	H1	H0
Acq. Mode B	5	–	–	–	S4	S3	S2	S1	S0
Display chapter (normal)	6	–	–	–	A4	A3	A2	A1	A0
Display chapter (supplm.)	7	–	–	CLUT SELECT	A4	A3	A2	A1	A0
Display (normal)	8	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display (news flash)	9	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control	10	STATUS $\overline{\text{BTM}}$/TOP	CURSOR ON	$\overline{\text{CONCEAL}}$ REVEAL	$\overline{\text{TOP}}$/ BOTTOM	$\overline{\text{SINGLE}}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
CLUT data 1	11	G3	G2	G1	G0	R3	R2	R1	R0
CLUT data 2	12	A3	A2	A1	A0	B3	B2	B1	B0
Active chapter	13	–	–	CLEAR MEM.	A4	A3	A2	A1	A0
Active row	14	–	CURSOR MOVE	INC BY ROW	R4	R3	R2	R1	R0
Active column	15	$\overline{\text{R16C}}$/ R16C	$\overline{\text{R16A}}$/ R16B	C5	C4	C3	C2	C1	C0

Table 5 Register map *(continued)*

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Active data	16A	D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)
Device status	16B	$\overline{625}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY
End of page flags	16C	8/30 ARRIVED	X/29 ARRIVED	X/27 ARRIVED	AC4	AC3	AC2	AC1	AC0

Notes to Table 5

1. – indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. All bits in registers R0 to R15 are cleared to logic 0 on power-up, except bits D0 and D1 of registers R1, R8 and R9 which are set to logic 1. The CLUT data (accessed from R11 and R12) is cleared to normal "level 1" colours.

Register description

R0 MODE - auto increments to Register 1

BOX HEADER	Selects automatic boxing of first 7 characters on display Row 0
BOX TIME	Selects automatic boxing of last 8 characters on display Row 0
POL	Selects polarity of STTV output or LFB and FFB input signals. (When POL = 1, then TCS will be positive-going syncs and LFB/FFB will be negative; when POL = 0, TCS will be negative-going syncs and LFB/FFB positive)
B.T.NUMBERS ENABLE	Selects blast-through numbers instead of supplementary background colour attributes
DISABLE HDR ROLL	Stops the display update of rolling time and green rolling header during page request when = 1. Time updates on page reception only
$\overline{\text{DEW}}$/FULL FIELD	Field-flyback or full channel mode
EXTN. PACKET ENABLE	Enables reception and storage of extension packets in 2 K x 8-bits per page when = 1
X24 POS	Automatic display of FASTEXT prompt row when = 1

R1 SYNC - auto increments to Register 2

T0, T1	Interlace/non-interlace 312/313 line or scan sync control
TCS ON	Text composite sync or direct sync select
VCR	Selects VCR mode for display PLL
DISABLE ODD/$\overline{\text{EVEN}}$	ODD/$\overline{\text{EVEN}}$ unconditionally forced low if = 1
AUTO ODD/$\overline{\text{EVEN}}$	If = 1 then ODD/$\overline{\text{EVEN}}$ output only active when no picture is present
FREE RUN PLL	Forces display PLL to free run at 6 MHz when = 1
VCS TO SCS	Connects VCS from video sync separator to display field sync detector to enable stable display status messages with 60 Hz rasters

R2 ACQ. CONTROL - auto increments to Register 3

START COLUMN	Start column for page request data
TB	Must be logic 0 for normal operation
ACQ. CCT	Selects one of five acquisition circuits
ACQ. $\overline{\text{ON}}$/OFF	Entire acquisition function turned off when = 1

R3 PAGE REQUEST DATA - does not auto increment

Table 6 shows the full register map for page requests. The mapping of Register 3 is dependent on the start column indicated in Register 2.

Table 6 Register map for page requests (R3)

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	$\overline{\text{CLEAR}}$ $\overline{\text{RX}}$	$\overline{\text{ROLL}}$	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0
7	CH4	CH3	CH2	CH1	CH0

Notes to Table 6

1. When the DO CARE bit is set to logic 1, this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0, the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
2. There are five versions of Table 6, one for each acquisition channel. This allows five simultaneous page requests.
3. $\overline{\text{ROLL}}$ set low to give rolling headers on page search.
4. $\overline{\text{CLEAR}}$ $\overline{\text{RX}}$ set low to clear old page on first reception.
5. Columns auto-increment on successive I²C-bus transmission bytes. Column 7 auto increments back to Column 0.
6. CH0 to CH4 are pointer bits (LSB to MSB) giving the current chapter address for that acquisition channel.

Where:

Page number

MAG	magazine
PU	page units
PT	page tens
$\overline{\text{HOLD}}$	set LOW to hold and not update page
CH	chapter address bit

Page sub-code

MU	minutes units
MT	minutes tens
HU	hours units
HT	hours tens.

R4 ACQ. MODE A - auto increments to Register 5

R5 ACQ. MODE B - auto increments to Register 6

These bits determine the type of acquisition to be performed by each of the five acquisition channels. H is Hamming and S is select. The four combinations are shown in Table 7.

Table 7 Truth table for acquisition Modes A and B

H	S	FUNCTION
0	0	7-bit plus parity
0	1	8-bit (no error checking)
1	0	8/4 Hamming checking over the full page
1	1	mixed 8/4 Hamming (Columns 0 to 7, 20 to 27) and 7-bit plus parity (Columns 8 to 9, 28 to 39)

R6 NORMAL DISPLAY CHAPTER - auto increments to Register 7

A0 to A4 Selects one of 32 chapters for display. This register is used for full pages of display, when the current display row bit is set to 0

R7 SUPPLEMENTARY DISPLAY CHAPTER - auto increments to Register 8

A0 to A4 Selects one of 32 chapters for display This register is used when the current display row bit is set to 1, for e.g. status messages on a text page

CLUT SELECT Determines which CLUT will be written to by Registers 11 and 12. If set to 1, access is to the supplementary display chapter colour entries

R8 NORMAL DISPLAY CONTROL - auto increments to Register 9

R9 NEWSFLASH/SUBTITLE DISPLAY CONTROL - auto increments to Register 10

PON Picture on

TEXT Text on

COR Contrast reduction on

BKGND Background colour on.

These functions have IN and OUT bits referring to inside and outside the boxing function respectively.

R10 DISPLAY CONTROL - does not auto increment

BOX ON 0	Boxing function allowed on Row 0
BOX ON 1-23	Boxing function allowed on Row 1-23
BOX ON 24	Boxing function allowed on Row 24
STATUS ROW $\overline{\text{BTM}}$/TOP	Row 24 displayed above or below the main text

R11 CLUT DATA 1 - auto increments to Register 12

R0 to R3	Red colour value
G0 to G3	Green colour value

R12 CLUT DATA 2 - auto increments to Register 11

B0 to B3	Blue colour value
A0 to A3	Address of colour entry

R13 ACTIVE CHAPTER - auto increments to Register 14

A0 to A4	Active chapter address for I²C-bus

CLEAR MEM.Clears the external memory to power-on state

R14 ACTIVE ROW - auto increments to Register 15

R0 to R4	Active row address for I²C-bus
INC BY ROW	When set the active address increments by row on R16A accesses instead of by column
CURSOR MOVE	When set the active I2C Row and columns are read and used to update the cursor position on the display

R15 ACTIVE COLUMN - auto increments to Register 16A/16B/16C depending on bits D6/7 of Register 15

C0 to C5	Active column address for I²C-bus
$\overline{\text{R16A}}$/R16B	Selects either Register 16A (read/write) or 16B (read only)
$\overline{\text{R16C}}$/R16C	Selects Register 16C (read only) or allows selection of Registers 16A or 16B

R16A ACTIVE DATA

D0 to D7 (R/W)	Data bits (read/write)

R16B DEVICE STATUS - does not auto increment

VCS SIGNAL QUALITY	Indicates that video signal quality is good and PLL is phase-locked to input video signal when = 1
TEXT SIGNAL QUALITY	If a good teletext signal is being received, then = 1
ROM VER R4-0	Indicates language/ROM variant. For Western European = 10000
$\overline{\text{625}}$/525 SYNC	If the input video is a 525 line signal then = 1

R16C END OF PAGE AND PACKET FLAGS - does not auto increment

AC0 to AC4	Set to 1 if an end of page has been detected in the corresponding acquisition channel
X/27 ARRIVED	Set to 1 if packet X27/0-1 and 4 arrives
X/29 ARRIVED	Set to 1 if packet X29/0-1 arrives
8/30 ARRIVED	Set to 1 if packet 8/30/0-3 arrives

Table 8 Crystal characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	-	1.7	-	pF
C0	parallel capacitance	-	5.2	-	pF
CL	load capacitance	-	20	-	pF
Rr	resonant resistance	-	-	50	Ω
R1	series resistance	-	20	-	Ω
Xa	ageing	-	-	±5	10^{-6}/yr
Xj	adjustment tolerance	-	-	±25	10^{-6}
Xd	drift	-	-	±25	10^{-6}

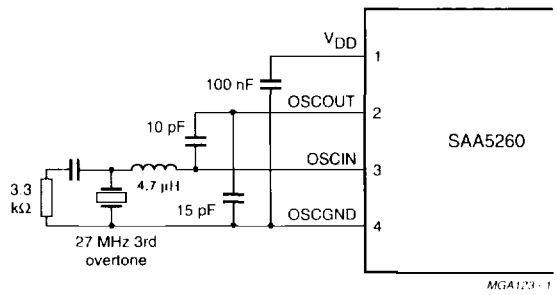


Fig.11 Crystal oscillator application diagram.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone, as shown in Fig.11. The crystal characteristics are given in Table 8.

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. For languages based on the Roman alphabet, the basic 96 character sets differ only in 13 national option characters. For the Western European version of SAA5260, these national option characters are shown in Table 9, with reference to their position in the basic character matrix illustrated in Table 10.

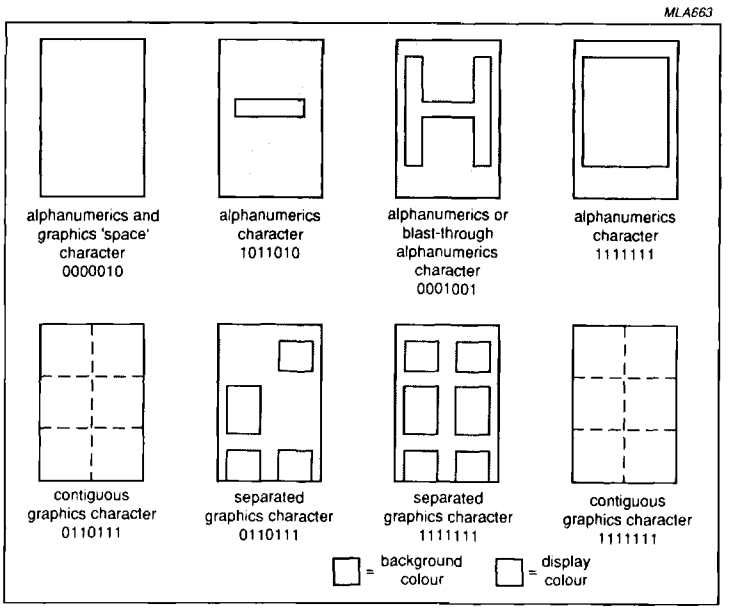


Fig.12 Character format.

Table 9 SAA5260P/E Western European national option character set

The SAA5260 automatically decodes transmission bits C12 to C14. Table 11 illustrates the 8-bit decoding of the character matrices.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

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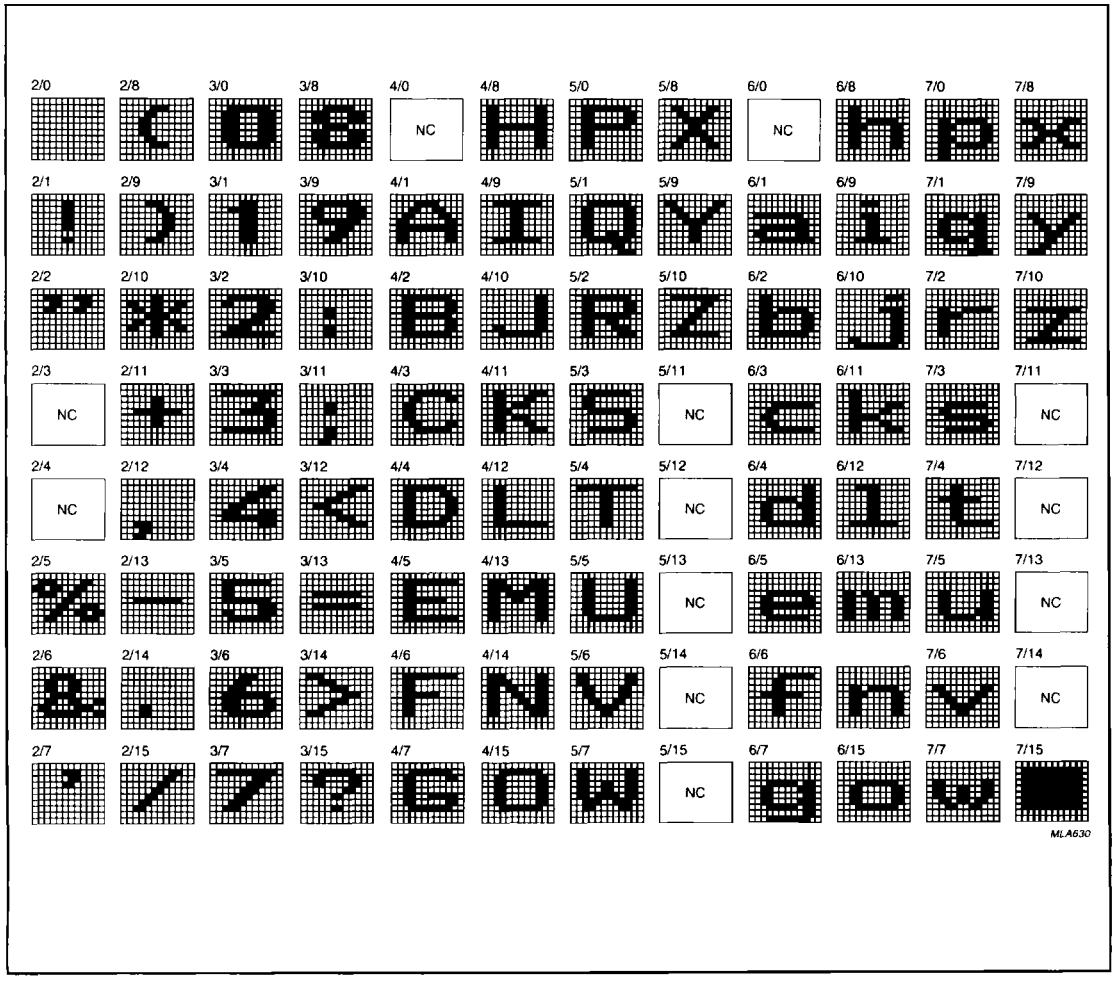
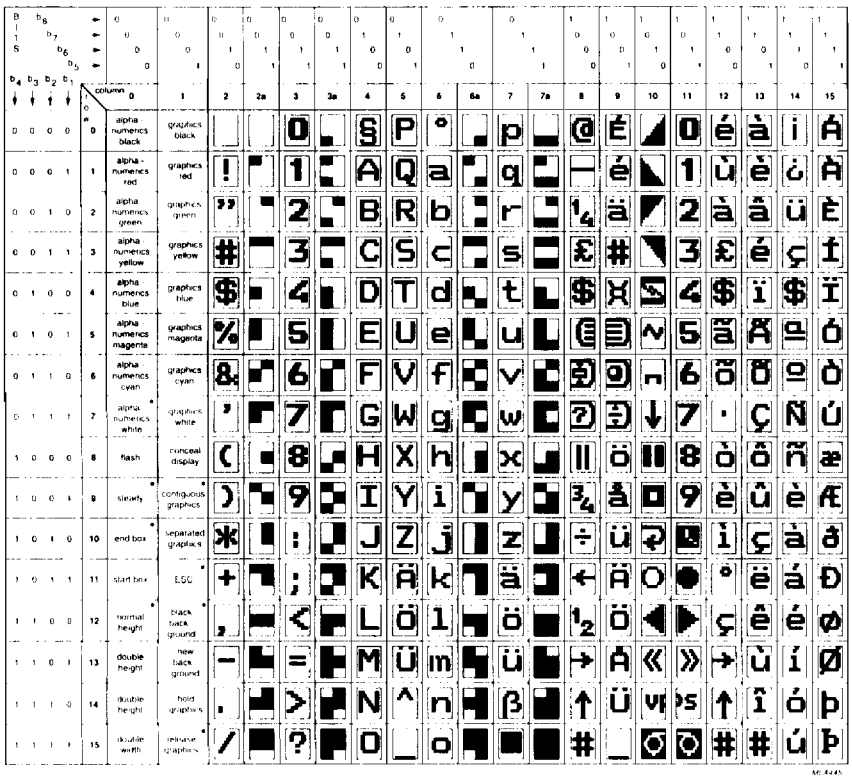
(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Table 10 SAA5260 Western European basic character matrix



Where: NC = national option character position.

Table 11 SAA5260P/E character data input decoding (Western European Version)



For character version number (10000), see Register 16B.

* These control characters are presumed before each row begins.

Notes to Table 11

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Columns may be referred to by columns and row, for example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. The SAA5260 national option characters are illustrated in Table 9.
5. Character 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5.
6. With bit 8 = 0, national characters will be decoded according to the setting of control bits C12 to C14 (see Table 9).
7. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.
8. Column 11 rows 0 to 7 are normally special attributes for setting the background colour. The numerals 0 to 7 are obtained instead when R0D3 is set to 1, to allow blast-through alphanumeric numbers in graphics mode.

Colour Facilities

Table 12 shows the format for both supplementary and normal page colour look-up tables (CLUTs). 12 bits are used for each colour entry. This allows the display colours to be chosen from a palette of 4096 different shades (16 levels possible on each of the R, G, B output pins from the internal DAC).

There are a total of 16 addresses in each CLUT, allowing each of the 8 foreground colour and 8 background colour values defined by the control characters to be assigned a particular shade, and separate colours to be assigned for normal and supplementary display pages.

On power-on, both CLUTs are cleared to full amplitude values corresponding to the R, G and B address inputs to give the normal 'level 1' display colours as shown in Table . They can then be re-defined by the microcomputer via the I²C-bus if required; registers R11 and R12 defining CLUT data and address, and R7D5 defining the CLUT to be used. R7D5 = 0 selects the CLUT for the normal page, while R7D5 = 1 selects the CLUT for the supplementary display page.

CLUT addressing and defaults

ADDRESS		MEANING	DEFAULT VALUE		
binary	decimal		R	G	B
0 0 0 0	0	BLACK background	0000	0000	0000
0 0 0 1	1	RED background	1111	0000	0000
0 0 1 0	2	GREEN background	0000	1111	0000
0 0 1 1	3	YELLOW background	1111	1111	0000
0 1 0 0	4	BLUE background	0000	0000	1111
0 1 0 1	5	MAGENTA background	1111	0000	1111
0 1 1 0	6	CYAN background	0000	1111	1111
0 1 1 1	7	WHITE background	1111	1111	1111
1 0 0 0	8	BLACK foreground	0000	0000	0000
1 0 0 1	9	RED foreground	1111	0000	0000
1 0 1 0	10	GREEN foreground	0000	1111	0000
1 0 1 1	11	YELLOW foreground	1111	1111	0000
1 1 0 0	12	BLUE foreground	0000	0000	1111
1 1 0 1	13	MAGENTA foreground	1111	0000	1111
1 1 1 0	14	CYAN foreground	0000	1111	1111
1 1 1 1	15	WHITE foreground	1111	1111	1111