DIGITAL COMPACT CASSETTE RECORDER

THIRD GENERATION DCC (reference set: DCC951)

Service
Service
Service

DIGITAL dcc COMPACT CASSETTE

Circuit Description

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PHILIPS

Preface

This circuit description is an add-on to the DCC Basics System description, Chapter 7 in the Audio Training Kit 1993.
In this publication the third generation DCC-chip set and mechanics are described. As reference set has been chosen: DCC951; but the heart of this set, the Digital compact cassette Deck Unit is an application which will be implemented in a lot of other Audio Systems.
This description is intended to be used by service trainers, service technicians and others who are interested in the applied technologies and it explains in a more extended way, a number of short instructions as those are laid down in the Service Manuals. Reference is made to Service Manual drawings and in steps the most important actions and applied technology are explained.

After the study of this description the service technician will be able to analyze the related to DCC occurring faults, which results in a quick diagnosing. So, via this publication, the reduction of the repair time can be realized.

To get familiar with set DCC951 the commercial leaflet has been included in the introduction chapter. After that the technical description starts.

Introduction

DIGITAL COMPACT CASSETTE RECORDER

DCC 951

900 SERIES "DIGITAL CONVENIENCE" DCC RECORDER

- **Direct digital recording**
- **Plays also Compact Cassettes**
- **Full 18-bit system**
- **Turbo drive**
- **Title recording**
- **Microphone input**
- **"System Intelligence" bus**

DCC951 DIGITAL COMPACT CASSETTE RECORDER

PHILIPS DCC: THE COMPATIBLE DIGITAL RECORDING SYSTEM

With the DCC 951, Philips proudly presents the Digital Compact Cassette (DCC) recording system. In the same way as Compact Disc has taken over from vinyl records, DCC will replace the Compact Cassette.

The DCC 951 records and plays back music digitally, using a new design audio cassette, running at normal Compact Cassette speed. High quality digital registration is achieved by Precision Adaptive Sub-Coding (PASC), which is optimally matched to the actual characteristics of the human ear.

Features of the DCC deck include direct digital recording with full 18-bit resolution, fast access to any music track thanks to Turbo Drive wind and rewind, sophisticated record editing and title recording. Plus, of course the high-convenience of the Philips 900 Series System Intelligence Bus.

Besides the new DCC cassettes, the DCC 951 also plays your existing - and valuable - collection of analogue Compact Cassettes. This autoreverse, full logic deck knows when you insert a Compact Cassette, and automatically switches over to its analogue playback head. Playback sound quality is high indeed, and there is a choice of Dolby B or C Noise Reduction.

A CLEAN, SLIMLINE 900 SERIES SYSTEM COMPONENT

Slimline design and unusually clean lines: these are the arresting visual impressions of the DCC 951. They are the results of ingenious engineering design. And they are supported by standards of sound quality and easy, speedy operation not achieved before, even in a DCC deck.

DIRECT DIGITAL RECORDING

A choice of optical and coaxial digital inputs allows direct recording from CD, satellite radio, or any other present or proposed digital audio source. Direct digital recording preserves all the sound quality of the original source, and no record level setting is needed.

"SET-AND-FORGET" LEVEL SETTING FOR EASY DIGITAL RECORDING FROM ANALOGUE SOURCES

For analogue inputs, record level setting is easy because of the ample room within the high dynamic range of the DCC system, and it is made easier by the DCC 951's Up/Down record level setting keys.

What's more, the optimal level for each source (CD, tuner and so on) only needs setting once, at which time it is automatically stored in memory. Thereafter, the DCC 951 always selects the memorized level at the same time as the recording source.

"APPEND" KEY FOR AUTOMATIC RECORD SEARCH.

The Append key is a powerful tool for setting your deck up for recording. Sequential pressing of this key takes your first to the start of the cassette, and then to the end of the last recorded track.

Append allows you to find and directly verify (Append-Play) and desired position to start a new recording. In record pause mode, you can then monitor the source to ensure errorfree recording. Further, Append guarantees correct sequential recording of track numbers and playing times.

RECORD EDITING

With the edit key, you control the way music programmes are recorded and the way tracks are numbered.

Edit lets you record a single programme on both sides of a cassette, or seperate programmes on the two sides, always with the option of rewinding automatically to the start of side A.

FULL 18-BIT SYSTEM

The full 18-bit resolution of the digital recording and playback circuits preserve all the dynamic range and resolution of the original music, without introducing the slightest hint of distortion. This, together with advanced PASC coding and decoding algorithms, which mirror the actual characteristics of the human ear, ensures superb digital sound quality for listeners.

State-of-the-art sigma-delta A/D and bitstream D/A converters safeguard the integrity of the analogue line inputs and outputs.

SPEEDY ACCESS WITH TURBO DRIVE

The DCC 951's Turbo Drive mechanism gives you far faster access times than a regular cassette mechanism. In conjunction with the DCC track finding system, this very quickly finds and locks on to any music track or the blank recording area.

TITLE RECORDING

The DCC 951 reads and displays the text information from pre-recorded DCC cassettes, such as album and track titles and the artistes' name.

What is more, the Title Recording feature lets you use either front panel or remote control to record the titles of tracks that you record yourself (maximum 40 characters). On playback, you will see each track title scroll into the deck's 14-character display when the track starts to play.

When you search through the tracks, you immediately see the titles on the display, so that you know for sure when you have found the one you want.

PERSONAL PRESETS

You can set up the DCC 951 in a choice of operating modes to save you trouble later on. Via the Presets key, the deck can be set for Autoplay (when a cassette is loaded) and Autostop: coaxial digital, optical digital for analogue inputs can be selected individually for the four sources (CD, Tuner, Aux 1 and Aux 2); and for CD Synchro operation in conjunction with the CD player.

ADVANCED PHILIPS TECHNOLOGY: THE DDU 2113 DRIVE UNIT

Heart of the DCC 951 is the high-performance DDU 2113 Drive Unit. Only 61mm high, this incredibly compact assembly contains the thin-film record/playback head unit with 2 x 9 digital and 2 analogue tracks, all digital circuits including the PASC encoder/decoder, the full logic controlled autoreverse mechanism with Turbo Drive and full record and playback control, and a smooth, motorized tray loader.

THE 900 SERIES "SYSTEM INTELLIGENCE" BUS

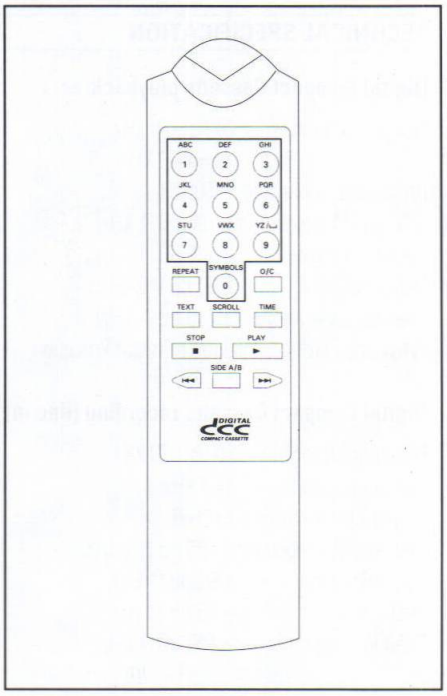
This DCC deck belongs to the Philips 900 Series of Hifi system range. And Series 900 breaks the mould of conventional Hifi system design. With characteristic symmetrical syling and firmly sensitive touch control. With insistence on userfriendly operation, based on a consistent control and display philosophy combined with the "System Intelligence" bus.

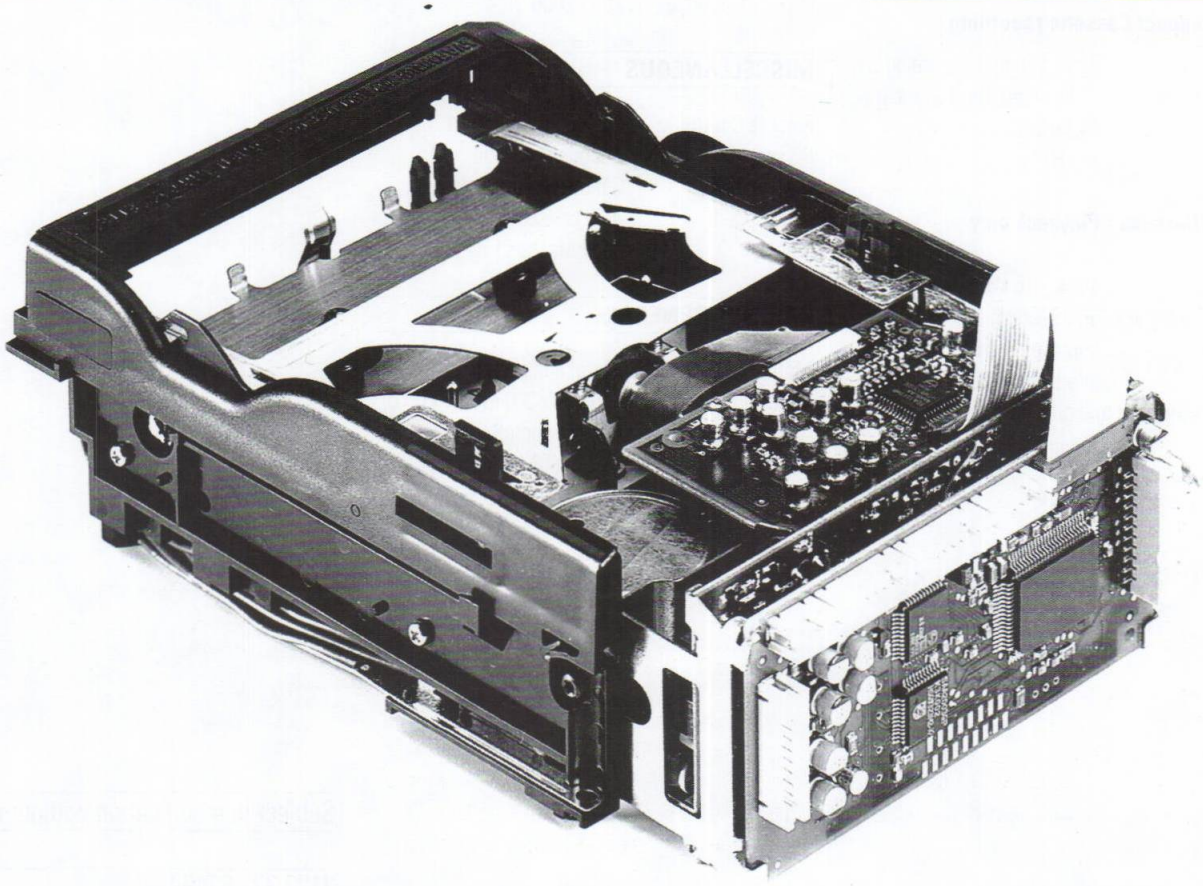
Through the 2-way "System Intelligence" bus, 900 Series system components do far more than respond to conventional remote control; they interact intelligently with each other.

Operation is extremely easy because the system components do most of the work themselves. The system's software clock/timer in the FT930 tuner, for example, easily and conveniently controls recording or playback on the DCC 951.

CHOICE OF DIRECT OR 900 SERIES REMOTE CONTROL

The remote control handset supplied contols virtually all deck functions, including direct track selection and title recording with the alphanumeric keys. Alternatively, play, next/previous, backward, forward, direction and stop can all be contrelled remotely via a 900 Series amplifier and the bidirectional ESI-bus.





DCC951 DIGITAL COMPACT CASSETTE RECORDER

TECHNICAL SPECIFICATION

Digital Compact Cassette playback:

Frequency Ranges	: 20 Hz - 20 kHz (fs = 44.1 kHz)
Amplitude Linearity	: ±0,05dB
S/N ratio (A weighed)	: ≥ 105 dB (1 kHz)
Dynamic range	: ≥ 100 dB (1 kHz)
THD + N	: ≥ 90 dB (10 kHz)
Channel separation	: ≥ 110 dB (1 kHz)
Wow and Flutter	: Quartz Crystal Precision

Digital Compact Cassette recording (line in):

Frequency Range	: 20 Hz - 20 kHz
Sample frequency	: 44,1 kHz
Amplitude Linearity	: ±0,1dB
S/N ratio (A weighed)	: ≥ 100 dB (1 kHz)
Dynamic range	: ≥ 92 dB (1 kHz)
THD + N	: ≥ 85 dB (1 kHz)
Channel separation	: ≥ 100 dB (1 kHz)

Digital Compact Cassette recording

	: Perfect Digital Recording.
Sample frequencies	: 32 kHz (satellite Tuner e.g.)
	: 44,1kHz (CD)
	: 48 kHz

Analogue Cassette : Playback only

Frequency Range	: 40 Hz - 16 kHz (CrO_2)
S/N ratio (A weighed)	: 55 dB (CrO_2)
Dolby B/C	: Improvement B : 10 dB Improvement C : 18 dB

Signal also supplied to digital outputs.

INPUTS

Analogue	: impedance 50kOhm
Digital coaxial	: acc. to IEC 958
Digital optical	: TOSLINK

OUTPUTS

Analogue	: 2 Vrms
Digital coaxial	: acc. to IEC 958

HEADPHONE

Load impedance range	: 32 - 600 Ohm
Output impedance	: 170 Ohm
Output voltage (L and R)	: Max. 5V Rms
Frequentie range	: 20 Hz - 20 kHz

MICROPHONE

Microphone impedance range	: 200 - 2000 Ohm

MISCELLANEOUS

Remote Control	: 20 key RC-5 infrared
RC socket	: ESI bus, 2x cinch
Mechanism	: 2 motor metal deck
Tape-speed	: 4,76 cm/sec
Display	: 14 characters FTD

CABINET GENERAL

Material/Finish	: Metal and polystyrene
Dimensions	: 435 x 90 x 300 mm (w x h x d)
Accesories	: Remote control, cinch cables (2x), digital connection cable

Subject to modification without notice

3122 321 52492

1 GENERAL

1.1 DCC recorders third generation.

In reference set DCC951 the third generation of DCC technology has been applied. This set can be split up in the electrical interface part and the tape drive part.
In the interface part the front control module and the power supply unit with in- and output modules are located.
The front control module concentrates on the tasks towards the user of the DCC-set, such as keyboard and remote control.
The tape drive part is a stand-alone DCC Module, which controls the DCC mechanism and the DCC ICs. It implements the DCC standard in such a way that the interactions of DCC and mechanical control are hidden for the front control module.
This DCC module is called "DDU" (Dcc Digital Unit).
The DCC Digital Unit (DDU-2113) consists of

- Motorized landscape tray-loader
- DCC high speed mechanism (CMRD tape deck).
- DCC electronics
- Standardized I/O's

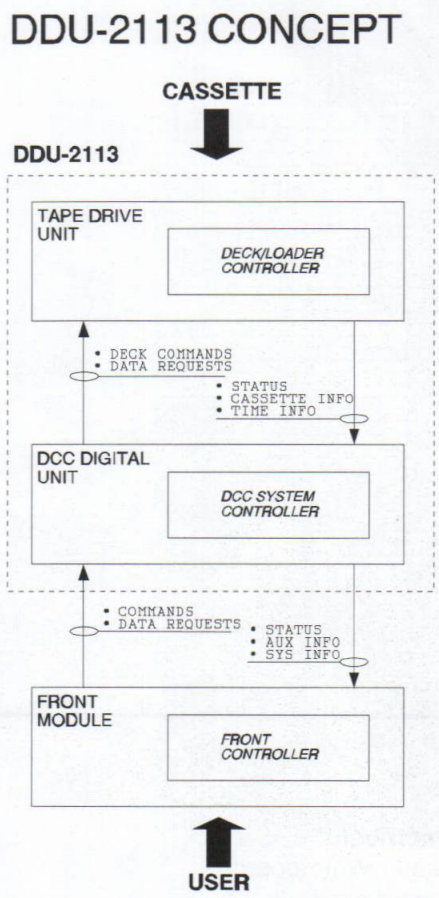


Fig. 1. Typical 3 part architecture of a DCC recorder

Because it is expected that this DDU module and/or derived versions of it, will be applied in many different audio sets the various functions of the tape drive part (= DDU module) will be explained in detail in this publication.

The complete DCC set can be seen as existing out of three main parts, shown on figure 1:

- The Front Module
- The DCC Digital Unit
- The Tape Drive Unit

The tasks of the Front Module are

- the dialogue with the user via keyboard or remote control,
- the dialogue with other audio components,
- controlling the DCC Digital Unit,
- showing the status of the system on a display and
- the set specific procedures such as sequence programming.

The Front Module communicates with the DCC Digital Unit by means of an easy and well defined interface. The Front Module controls the communication to the DCC Digital Unit.

The DCC Digital Unit provides all audio inputs and outputs, it starts the PASC and Drive processing and it controls the Tape Drive Unit mechanics. It accepts its commands from a front controller via an interface. This module acts as the master for the Tape Drive Unit. The microprocessor of the DCC Digital Unit takes care of realization of the DCC system standard regarding auxiliary and system information generation (sub-code) and handling and control of the IEC958 interface standard.

The Tape Drive Unit handles all aspects around the cassette, deck and loader. It provides means for recording of DCC cassettes and playback of DCC and compact cassettes in such a way that specific hardware and timing aspects of the mechanics are hidden for the DCC Digital Unit, which controls it.

The electrical and control interface of the Tape Drive Unit gives the possibility to communicate with the controlling DCC Digital Unit and passes information on the loaded cassette to it.
The DCC Digital Unit remains the master of the Tape Drive Unit interface.

DDU: DCC DIGITAL UNIT

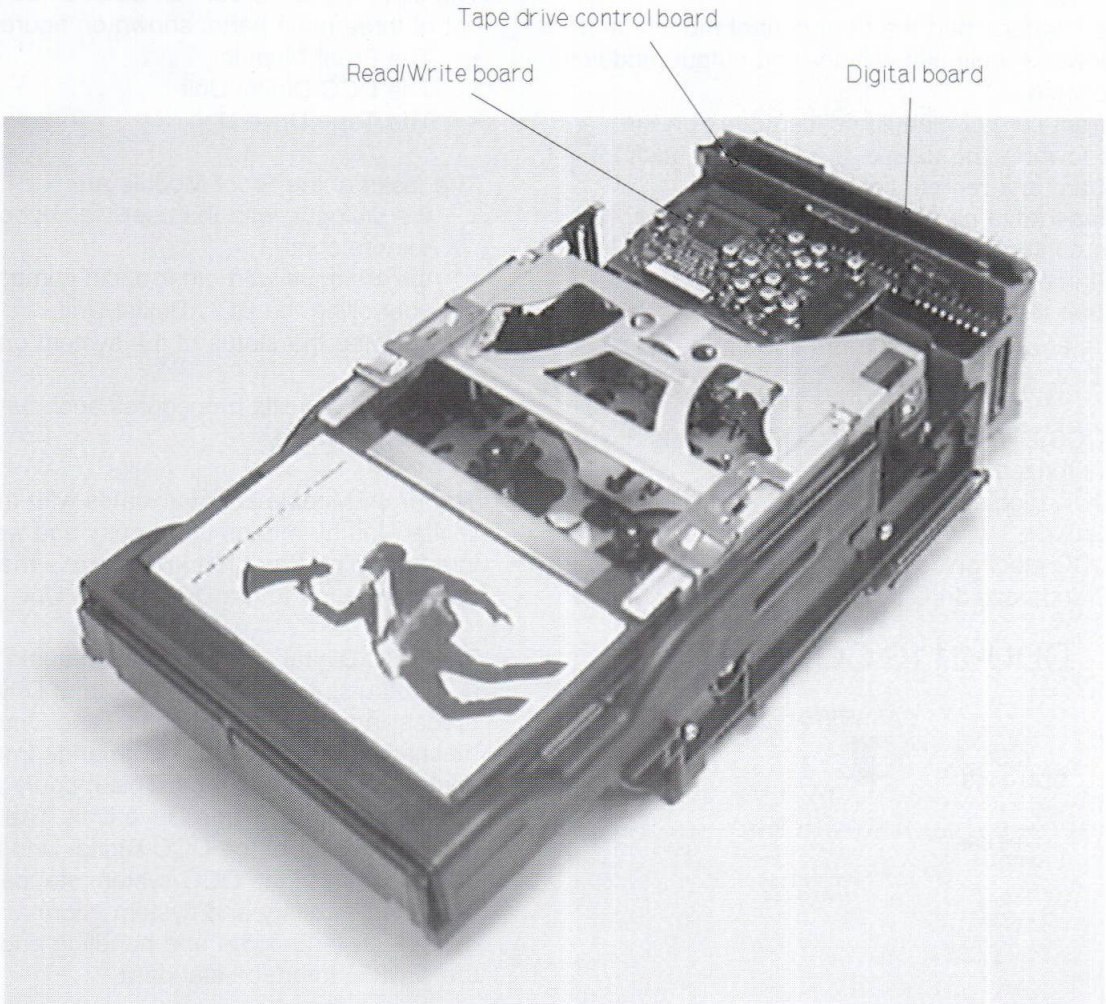


Fig. 2 DCC Digital Unit 2113

The DCC Digital Unit 2113 consists of:

Mechanical
Loader mechanism
Tape deck mechanism

Electrical
Read / Write board
Tape drive control board
Digital board

The functions performed by the DDU module are:

- Control of the tape drive module in order to:
  - fast transport the tape (wind/rewind)
  - open/close the loader
- Playback of:
  - 2-sector pre-recorded DCC cassettes
  - 4-sector pre-recorded DCC cassettes
  - Consumer recorded DCC cassettes
  - Analog compact cassettes
- Main data and/or auxiliary recording of:
  - DCC user tapes
  - DCC super user tapes
- Extended auxiliary channel marker recording support
  - Start marker recording
  - Skip marker recording
  - Reverse marker recording (including reverse lead in)
  - Next sector marker recording
  - Stop marker recording
  - Home marker recording
  - Use again marker recording
  - Lead in recording
  - Marker erasing
  - Blank/append search
  - User character recording
- Supplying the front controller module with data about:
  - System error codes and user error codes
  - Current status of the DCC digital module
  - Auxiliary information
    - Marker ID's
    - Track/Index/Chapter number
    - Absolute/Track time and remaining time
    - First/Last track
    - User characters
  - System information
    - Album title
    - Artist name (credits)
    - Current track
    - Sung text
    - Track list
  - Tape drive module tacho time
  - Cassette switches, tape type and tape length
  - Tape counter
  - Software version digital module and tape drive module
- Service support
  - Channel select for eye pattern output
  - Error indication per track
- Initialization
- Record pause
- Auxiliary channel renumbering
- Next/previous search
- Direct access search (TOC based)
- Absolute time estimation during search/wind
- AMS on ACC
- Analog audio inputs and outputs
- Digital audio inputs and outputs according to IEC958
- Full IEC958 user channel support during recording and playback
- PASC processing on all sampling frequencies, 32 kHz, 44.1 kHz and 48 kHz
- SCMS support
- Tape counter reset
- General system reset
- Audio output mute/fade and record mute/fade
- Source selection
- Power failure handling
- Standby handling
- Sector selection (A, B, C, D)
- Level meter support
- AD/DA control

1.2 Block diagram of the DCC Digital Unit Module (DDU)

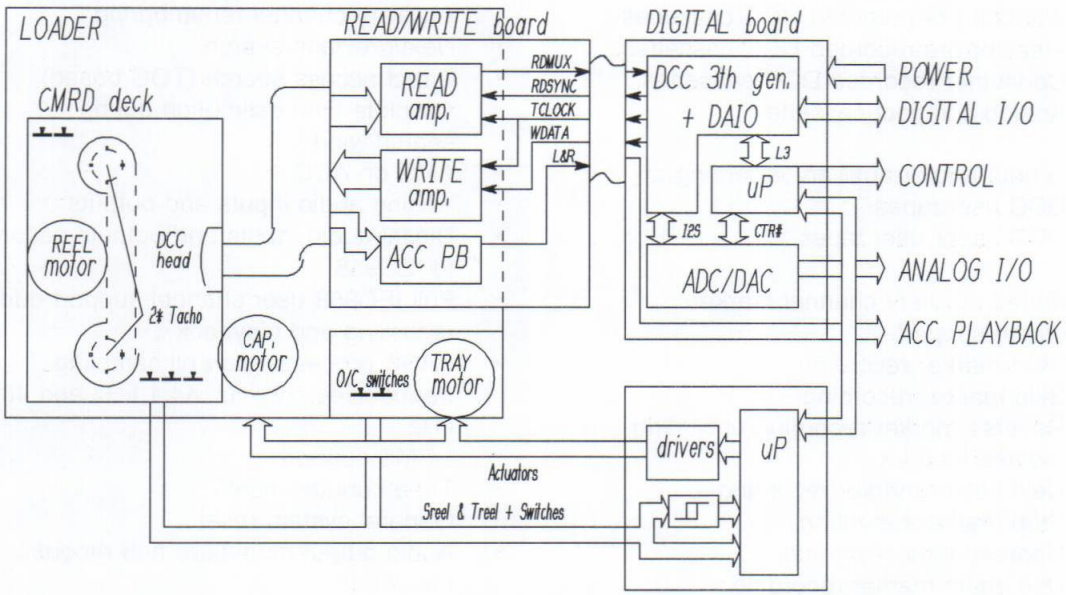


Fig. 3. General Block diagram of the DCC Digital Unit DDU

In the diagram of figure 3 the DDU Module has been drawn in functional blocks. Also the connections to the rest of the set (the interface part) are gathered and shown. These are:

- Power supply.
- Digital I/O (IEC958 in- and outputs to the optical and coaxial units)
- Analog I/O (ADC input; DAC output)
- Control bus; a bidirectional synchronous serial communication between the apparatus (master) and the processor on the digital board (slave).
- ACC playback output (L + R).

Other blocks in figure 3 are

- Digital board with µP,
- Read/Write board,
- Loader with CMRD deck,
- Tape Drive board with µP.

In general the signal flow can be described as follows:
When the module is in Recording mode:
In the digital board the input signal (Digital I/O or Analog I/O) is converted into digital format of WDATA and clocked by TCLOCK. This signal is fed to the write part of the Read/Write board, where the signal is split up into 9 channels for the DCC head.
In Read Mode and a DCC cassette is inserted, the 9 DCC head tracks deliver digital signals to the read part of the Read/Write board. After amplification, the signals are multiplexed into the RDMUX (Read multiplexed) signal, which is fed to the Digital board to be converted into the Digital- and Analog I/O output devices. The read multiplex operation is synchronized by the RDSYNC signal delivered by the digital Board.

When in Read Mode an analog compact cassette (ACC) is inserted, than the analog head tracks deliver the Left and Right analog signals to the ACC Play Back part of the Read/Write board and the analog is forwarded to the ACC PlayBack output devices.
The Tape Drive board actuates a.o. the capstan- and reel motor. The pulses of the Sreel (Supply reel) and Treel (Take up reel) indicate the turning speed of each reel. With the deck and loader switches, the various positions and cassette variations are defined to tape drive processor.

1.3 Block diagram DCC951

On the more extended block diagram of DCC951 (see figure 4 on next page) the various blocks and their interconnections are shown.
These blocks belong to the electrical interface part or to the tape drive part (DDU Module).

To the electrical interface part belongs:
- Front panel with the Control and Display functions;
- Input/output panel with Power supply and Analog output stage;
- Microphone and Headphone panel with the Microphone pre-amplifier and the headphone amplifier.

In the tape drive part is found:
- CMRD tape deck mechanism and Loader;
- Read/Write panel with read/write functions;
- Digital panel with the function to control the digital signal (DCC signal processing);
- Tape drive panel with the function to control the tape deck mechanism.

The signals between the various boards are found more detailed. Notice the heart beating function of the 3 μP's:
- Main μP (Digital board μP)
- Control & Display μP,
- Tape Drive μP.

These 3 processors are connected with each other via bus systems.
An important bus structure is the L3-bus. This bus is found between DRP, ADAS3, Port expander IC, SFC3, DAIO and Main μP. This is the control bus concerning the main activities of the DCC signal.
The DCC data are forwarded via the SB-I^2S and I^2S bus.

- DRP = DRive Processor. In the drive processor Digital read signal is EQualised (DEQ) and the read and write signals are both realized via Tape Formatting & Error correction (TFE).
- ADAS3 = ADaptive Allocation & Scaling for PASC coding of the DCC signal (only in Write mode active).
- SFC3 = Stereo Filter and Codec IC for PASC coding and decoding (in read and write mode). Sub-band filtering and audio frame coding in the PASC system are processed in this integrated circuit.
- DAIO = Digital Audio Input Output circuit.

1.3.1 Operation modes

There are four (basically different) operating modes in the DCC recorder:
- Data playback, Aux playback
- Data record, Aux record
- Data playback, Aux record
- ACC playback

In the next paragraphs these modes and their actions are explained.

1.3.1.1 Data playback, Aux playback

The head signals are first fed to the read amplifier (TDA1317), where they are amplified, filtered and supplied to a multiplexer. The output signal of the multiplexer (RDMUX) contains the information of the 8 main data tracks and the ninth AUX channel, and is passed on to the DRP (SAA2023). The DCC Drive Processor (DRP) reconstructs the original digital head signals, and after digital equalizing and Error correction procedures, together with DRAM IC MN4C4256, the digital data are recovered and demodulated from 10-to-8 bits. Via the sub-band interface all signals are formatted to the subband serial PASC data bus. This 'SB-I^2S-Bus' forwards the signal to the SFC3 (SAA2003). The Stereo Filter and Codec IC recovers the frames of data from the DRP. The PASC decoded sub-band samples are reconstructed by the sub-band filters into a single complete digital audio signal (SDA2). Sub-code information (Sub-code = System information + Auxiliary information) goes to the main microprocessor via the L3-Bus, (also connected to SFC3). The ADAS3 IC is inactive in this operating mode. The audio broadband signal is transferred via I^2S-interface to the DAIO (TDA1315), and via a port extender to the DAC (TDA1305T). The DAIO, together with sub-code information of

the main microprocessor, generates an IEC-958 signal, which is output via DIGITAL OUT. The D/A converted audio signals LEFT and RIGHT go to the appropriate analog outputs via buffer amplifiers.

1.3.1.2 Data record, Aux record

In this operating mode, the audio data either reach the DAIO directly via DIGITAL IN or OPTICAL IN (digital source), or are first digitized by the ADC (SAA7366) in case of an analog source. Via I^2S bus the digital audio data are passed to SFC3. Here, the broadband signal is separated into 32 subbands for left and right channels and a PASC frame is generated.
During PASC encoding the adaptive and scaling circuit (ADAS3) calculates the required accuracy (bit allocation) and scale factors of the PASC subband samples. The subband samples are transferred to ADAS3 via FDAI input port. The ADAS has to collect a complete frame of subband data before the allocation and scale factor information can be calculated. To have that information available in the same time frame as the audio samples are at the output, the subband filtered samples are delayed. (Dependant to the audio sample rate of 32, 44.1 or 48 kHz.) The delayed samples are passed to the codec part of SFC3 on the FDAO output port. This bus between SFC3 and ADAS3 in the recording mode is called the filtered data interface.
For every PASC frame the ADAS3 calculates a bit allocation and a scale factor table which is transferred to the SFC3. Once scaled the samples are re-quantized to reduce the number of bits to correspond with the allocation table, as calculated.
Synchronization, allocation and scale factor are added in SFC3 to provide a fully PASC data signal. These frames of data are now via 'SBI^{2}S-Bus' sent to the DRP.
In the DRP the subband samples are received in the subband serial PASC interface.
In the recording mode Tape Formatting and Error correction (TFE) part of this IC, the C1 and C2 error corrections are encoded and the signal is formatted for tape transfer.
The sub-code data come via the L3-Bus to the main microprocessor. Finally, the tape frame data are passed on serially to the write amplifier (TDA1319T), which drives the write heads accordingly.

1.3.1.3 Data playback, Aux record

This operating mode is a combination of the modes described above, and is used for (subsequent) deletion or writing of markers on the AUX track. The DRP continuously sends sysinfo data to the main microprocessor, and simultaneously generates AUX tape frames. The tape frames generated by the DRP are taken in serial form via WDATA to the write amplifier, which drives the AUX write head accordingly.

1.3.1.4 ACC playback

The analog head signals are first amplified by the read amplifier, and linearised by a magnetic feedback loop. A further filter stage ensures an ideal frequency response. The analog signal is then fed to the Dolby IC CXA1331S, and any distortion is corrected. The audio signal then goes via an amplifier stage to the ADC, where it is digitized. The DAIO generates (with the main microprocessor) an IEC958 signal, which is output via IEC OUT to DIGITAL OUT. The digital audio data are passed on to the DAC via the I^2S-interface of the DAIO, D/A converted, and taken to the appropriate analog outputs via buffer amplifiers.

DCC HEAD

READ/WRITE

DIGITAL

IN/OUT

VARIABLE HEADPHONE

DRAM 7631 MN42C4256 A0-A8 D1-D4

DRP 7630 SAA2023 WDATA TCLOCK RDSYNC RDMUX SPEED L3MODE L3CLK L3DATA L3REF L3INT SBDIR SBDA SBCL SBWS SBEF

ADAS3 7600 SAA2013 L3MODE L3CLK L3DATA FDAI FDAO FDWS FDCL FSYNC FRESET FDIR LRMODEC LRCLKC LRDATAC

SFC3 7610 SAA2003 SBDIR SBDA SBCL SBWS SBEF FDAO FDAI FDWS FDCL FSYNC FRESET FDIR LRMODE LRCLK LRDATA DEEM1 DEEM2 ATSB SWS SCL SDA1 SDA2

DAC 7760 TDA1305T DEEM1 DEEM2 ATSB DACL DACR SDDAC SWS SCK MSUB NMUTE

ADC 7780 SAA7366 SDAD SWS SCK LEFT IN RIGHT IN

DAIO 7620 TDA1315 SDA2 SD WS SCK L3MODE L3CLK L3DATA OPT_IN COAX-IN IEC_OUT

L3-BUS

SB I2S-BUS

I2S

CONTROL2 CONTROL1 CONTROL0 DAC CONTROL

7730 L3DATA L3DATA_IN L3DATA_OUT SDA1 SD SDAD SDDAC SDA2 SD

24,576 MHz 22,5792 MHz

W0-7, Wx

R0-7, Rx

A1,A2

TA1,2 & TA8,9

7882 WRITE AMPL. TDA1319T WDATA WCLCK

7805 READ AMPL. TDA1317 RDCLCK RDSYNC RDMUX

FILTER

7860 ANALOG PLAYBACK EQUALIZATION 70/120 uS

CHROME

TAPE-DRIVE

7500 TAPE DRIVE UP P87C52EBPN N_FAIL_P MSYNC RXD TXD RESET_UP N_DCC_REC_PROT DRIVER_S0/S1/S2 WIND_SPEED S/T REEL SWITCHES N_SOLP N_SOL N_CAPON

7700 MAIN UP UPD78P056GC MSYNC RXD TXD RESET_UP N_DCC_REC_PROT L3MODE L3DATA_OUT L3DATA_IN L3REF L3INT L3_RCV SLAVE-OUT SLAVE_IN MESSYNC NRESET CLOCK HOLD

7580 7570 7505 7510 DC DC

SOLENOID CONTROL PLAY MAG

CAPSTAN MOTOR CONTROL SPEED

M TRAY MOTOR M81

M WIND MOTOR M101

SOLENOID L101

M CAPSTAN MOTOR M102

DECK & LOADER SWITCHES

TRAY IN SW81

DCC CASSETTE PRESENT SW101

DCC RECORD PROTECT SW102

DCC TAPE LENGTH HOLE3 SW103

DCC TAPE LENGTH HOLE4 SW104

DCC TAPE LENGTH HOLE5 SW105

PLAY POSITION SW110

CRO2/TRAY OPEN SW111

CASSETTE PRESENT SW112

TACHO SUPPLY REEL

TACHO TAKE-UP REEL

CMRD/LOADER

7180 DOLBY NR CXA1331S LINEOUT1 LINEOUT2 PBIN NRSW LEVEL MODE

7806 EEPROM ST24C02A SCL SDA

7800 CONTROL & DISPLAY UP TMP87CP71F SLAVE-OUT SLAVE_IN MESSYNC NRESET CLOCK HOLD DOLBY_ON_NOFF DOLBY_B_NC LEVEL RESET NON_0FF_SUPPPLY ESI IN ESI OUT

7801 RESET MN1382-S

7820 IR RC5

7805 DISPLAY

18X 8MHz

CONTROL _ DISPLAY

POWER SUPPLY

KILL LEFT RIGHT

7001-2B LM833

7001-2A LM833

7400-2A NJM4556

7400-2B NJM4556

HEADPHONE OUT

ANALOG OUT LEFT

ANALOG OUT RIGHT

LEVEL

7455-2B NJM4560

7455-2A NJM4560

7451 MC74HC4051

7452 MC74HC4051

7201-2A MC34082

7201-2B MC34082

7200 MC74HC4052

ON DISPLAY PANEL

MICRO

7415 LM833

MICRO IN

ON HEADPHONE PANEL

7050-2A LM833

7050-2B LM833

ANALOG REC IN

OPTICAL IN

DIGITAL IN

DIGITAL OUT

IN OUT ESI

N_FAIL_P +5V +10VD +10VA -10VA +5Vper +5VD +5VA NON_0FF_SUPPPLY VFTD VAC1 VAC2

7921 7900 7920 7940

MAINS TRAFO VOLTAGE SELECTOR MAINS FILTER MAINS

Fig. 4. Block diagram DCC951.

HAS1142 9422

CIRCUIT DESCRIPTION 16

EXPLODED VIEW TAPE DECK

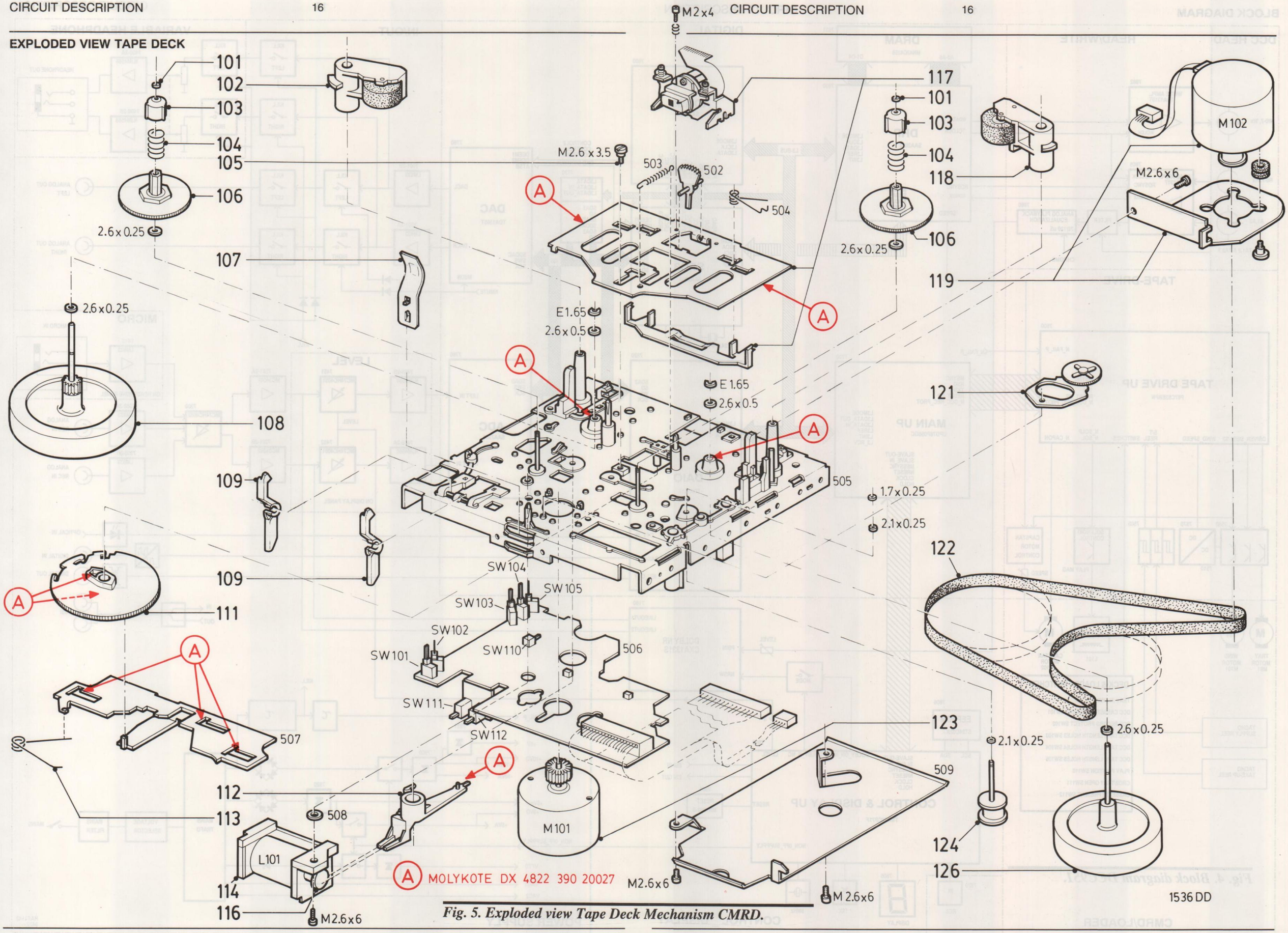


Fig. 5. Exploded view Tape Deck Mechanism CMRD.

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2 TAPE DRIVE PART MECHANICAL

The tape drive part consists of the loader part and the CMRD high speed DCC tape deck mechanism. The loader is a Landscape Tray Loader (LTL). Other loader types can be applied in other sets, more details about loader can be found in concerning service manuals. In this description only attention is paid to the tape deck drive mechanism part. In figure 5 the Exploded view of this CMRD deck has been shown.

The deck is the 'CMRD' deck, with all DCC switches and on the supply and the take up reel a tacho generator (6 pulses/rotation). The wind motor is suitable for high speed winding (50 x the normal play speed).
By use of the software information from the reel tachos there is no need for a quick reverse sensor to indicate tape end. With the information from the tacho reels the speed will be adapted at the moment the tape end approaches.

2.1 Head support

FIRST OF ALL A FEW SERVICE HINTS CONCERNING THE HEAD SUPPORT:

- Do not demount head support assembly, (head indentation)
- How handling DCC head

2.1.1 The head indentation

The head support, item 117 on the exploded view, is an assembly which carries the DCC-head. This DCC-head is in the factory adjusted on indentation depth. It is advisable to keep item 117 mounted.
This head support assembly is drawn separately in exploded view form in figure 6 to make ease recognizing of parts possible. It consists of command lever item 117B, head support item 117A, head item 501 (A to E) and cog item 502.

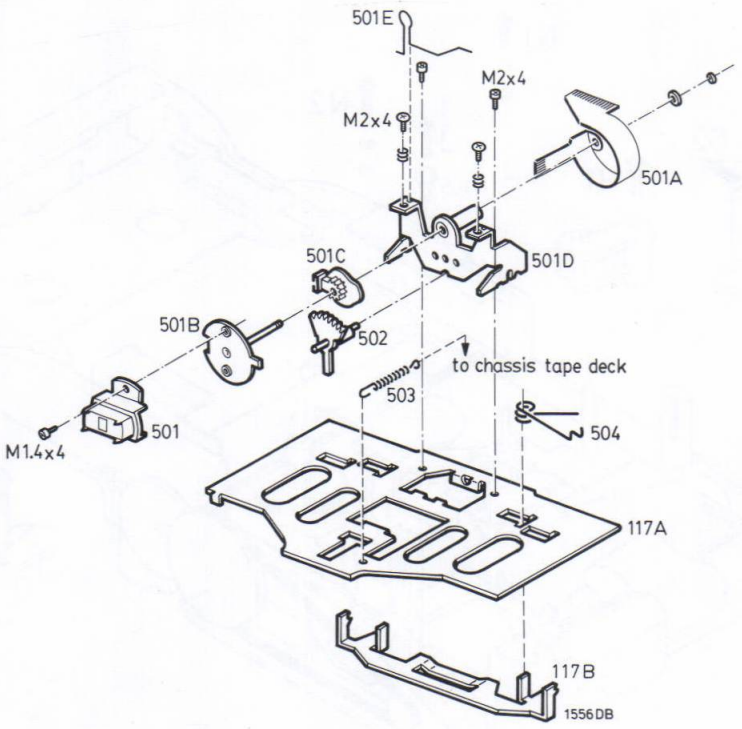


Fig. 6. Head support assembly.

NOTE: The positioning of the cog (item 502) and gearwheel (item 501C) is very critical too. (Head positioning in "A" sector and "B" sector mode.) In case item 502 deviates from its original position the head rotation by 180 degrees will not be obtained. The result is bad functioning in reverse or "B" sector mode.

2.1.2 Handling DCC-Head

CAUTION: Each head-device is suspectable to electrostatic voltage higher than 150Vdc! The head is protected against external electrostatic charging by connecting the head flexible cable to the read/write board. Before disconnecting the cable, always place the deck on a bench with required electrostatic discharging measures taken and wear electrostatic discharging band. Moreover, always mount the short-clip on the flexible cable removed. See figure 7. Action G3.

The head is also suspectable to strong external magnetic fields and the analog output may be affected.
DO NOT USE HEAD DEMAGNETIZER, MAGNETIC SCREWDRIVER OR DEMAGNETIZER CASSETTE!

Also in figure 7 the way how to loosen the head flexible cable is shown by action G1 u/i G3.
Pay attention to connector 1800. The fixation part of the connector, which will be moved by action G1, should be shifted over a very small distance. Otherwise the detentions of that part are destroyed.

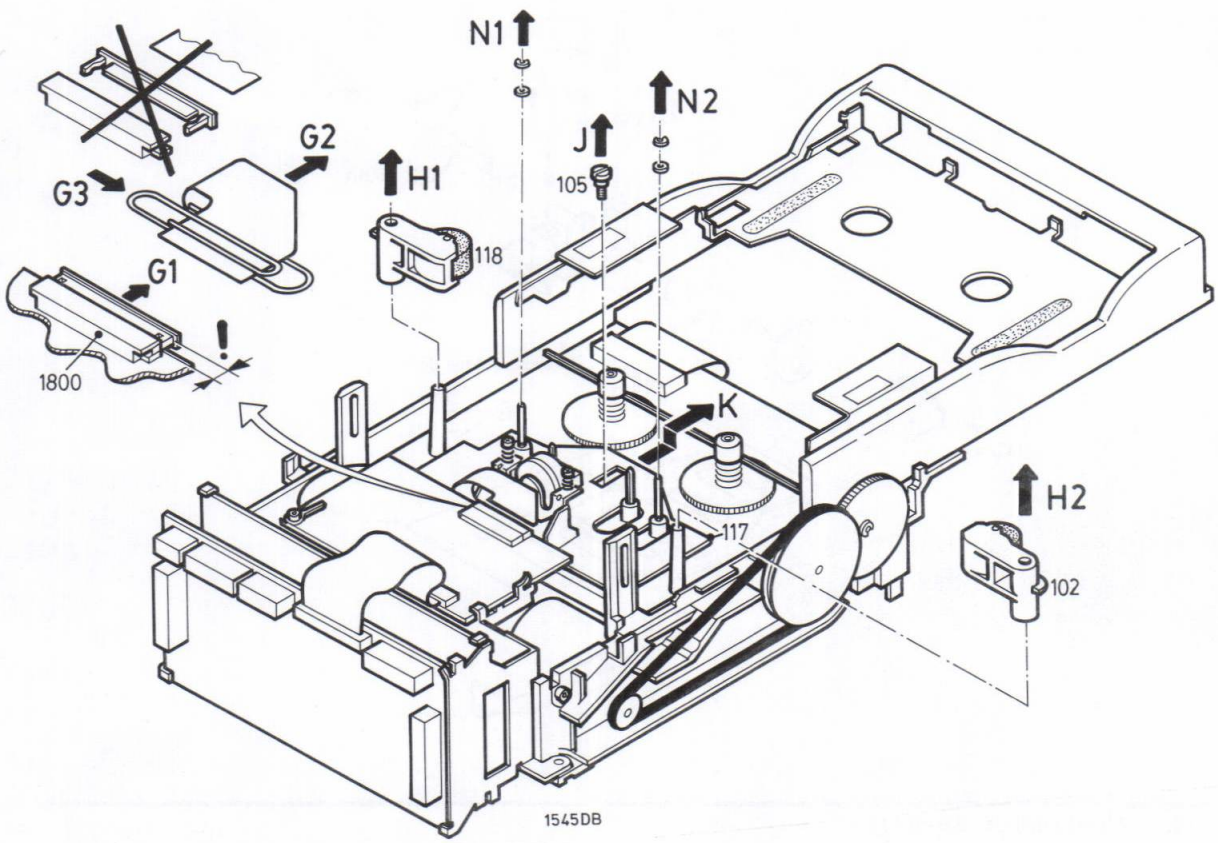


Fig. 7. Details of loosening head flexible cable.

2.2 Command gearwheel

2.2.1 Moving headsupport

All mechanical positions of the headsupport are achieved by the flywheel rotation (item 108). The gearwheel on this flywheel drives the command gearwheel (item 111) which positions, via cams at the bottomside, bracket item 507 (explanation follows). Via the cam on the top side (see exploded view, figure 5; item 111), the headsupport assembly item 117 is moved. By turning the command gearwheel the headsupport assembly (via a bent part of support-bracket 117A) is driven inside. By this movement the headsupport with head and pinch rollers are also moved towards tape and capstan. Dependant on the position of bracket 507 the left or the right pinch roller, by means of corresponding pinch roller spring, indicated with 504, is pressed against its capstan.

Is the bracket 507 near to the left pinch roller (item 102), spring 504 hooks onto the bracket of that roller and moves the roller against the capstan (item 108). In that position of 507 the right-hand spring 504 misses the hook of bracket 118, when head support assembly is moved inside, so the right-hand pinch roller does not come against capstan 126. Is bracket 507 moved to the right-hand pinchroller than that roller is brought against the capstan and than the opposite left roller will be free.
Also the cog (item 502) has been moved by item 507. This cog rotates via item 501C the head. With this movement the "forward" and "reverse" head positions are obtained.

The release of the command gearwheel is done by solenoid coil L101 with bracket item 112. Both positioned at the bottom side of the tape deck mechanism. For the timing of the solenoid pulses see Control timing charts paragraph 3.3.3.

2.2.2 Stop position

In figure 8 the Stop position of the gear wheel is shown. When L101 is activated, bracket 112 will no longer block gearwheel 111, but move this gearwheel a little bit counterclockwise and than it snaps into the capstan gearwheel. If the solenoid is activated the guiding pin of item 507 will come into the FWD mode (forward). See figure 9.

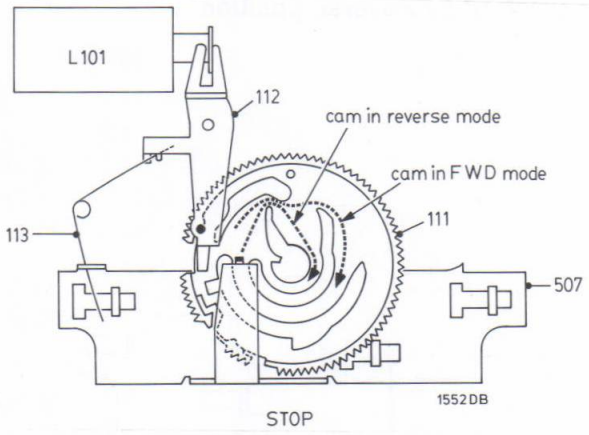


Fig. 8. Command gearwheel in Stop mode.

2.2.3 Play Forward position

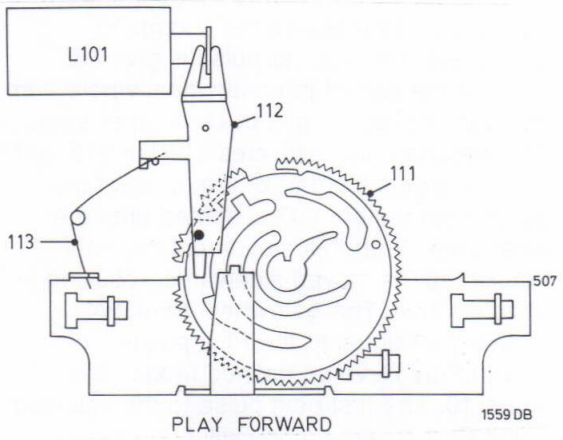


Fig. 9. Command gearwheel in Play Forward.

The gearwheel is driven by the capstan gearwheel approximately for 3/4 quarter part to the first following open part in the gearwheel and there it stops and item 112 blocks the gearwheel. The guiding pin of bracket 507 is driven into the mid track on command gearwheel 111. The mechanism is in Play forward mode. Via the force of spring 503 the head support assembly is pressed against the cam on top of the command gearwheel. In case the solenoid is activated in Play mode the command gearwheel will be released and bracket 112 slaloms through the mid opening (search position) forced by spring 503, until the command gearwheel reaches the stop position and is blocked again.

2.2.4 Play Reverse position

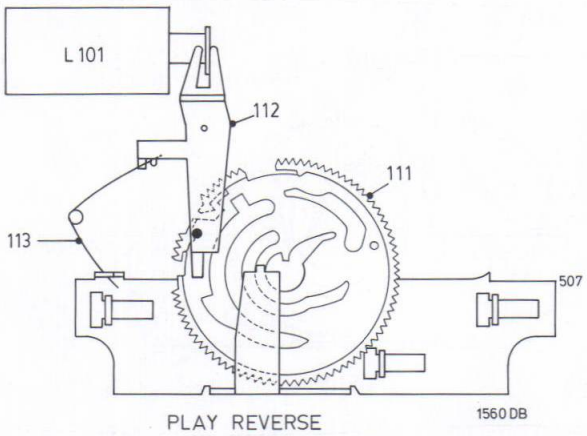


Fig. 10. Command gearwheel in Play Reverse.

To obtain the Play reverse mode the first solenoid pulse releases the command gearwheel. The second pulse is given is given in the part of the gearwheel where item 507 can choose for mid track or inner track. This second pulse activates bracket 112 and with the extension part of that bracket the guiding pin of item 507 is shifted onto the inner track. With this movement the total bracket 507 is moved sidewards, resulting in head rotation. The gearwheel turns 3/4 quarter part equal to the Play position but now in Play Reverse defined mode. See figure 10. The first next pulse to the solenoid in the Play reverse mode will bring the mechanism back again into the stop mode in the same way as described in the play forward mode.

2.2.5 Search "A" head position

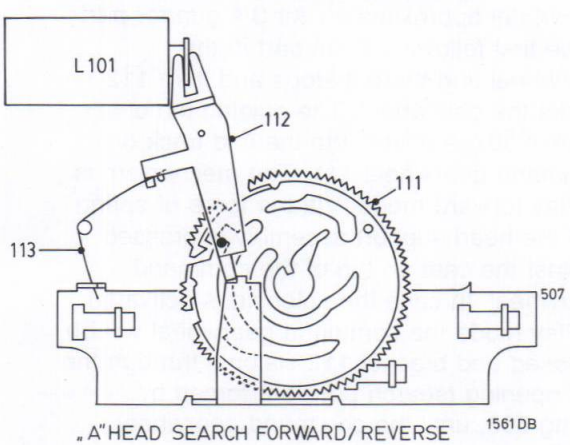


Fig. 11. Command gearwheel in the "A" head position Search Forward or Search Reverse.

To get from Play forward into the "A" head search forward or reverse mode the following actions are made. Mechanism in Play forward means that guiding pin 507 is in mid track. At the moment there is a first pulse from the solenoid, bracket 112 will release command gearwheel. When the solenoid remains activated the bracket 112 is driven to the inside of its cam and instead of a slalom near the search opening in the command gearwheel, now the bracket locks against the nock on the cam. As long as the solenoid is activated this position is kept. As the gearwheel has made a small rotation the head support assembly 117 is kept very near to the tape and search mode has been obtained.
Depending on the direction of the winding motor the forward or reverse Search mode is actual. See figure 11.

2.2.6 Search "B" head position

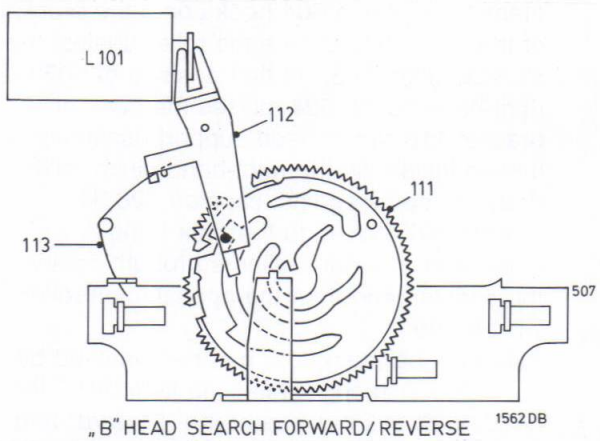


Fig. 12. Command gearwheel in the "B" head position Search Forward or Search Reverse.

The same principle as described before is used when coming from the reverse play mode into the "B" head search position. See figure 12. Via 507 is the head in the "reverse" or B-head position. As long as the solenoid is actuated this search mode will be kept as described in "A" head search mode.

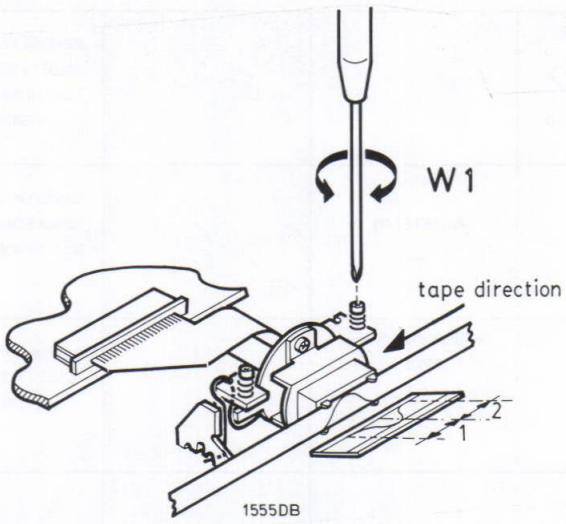
2.3 Azimuth adjustment

With the introduction of FATG (Fixed Azimuth Tape Guides) combined with ALP (Azimuth Locking Pins) the tape is forced to pass the head in vertical position. So the adjustment of the Azimuth has been changed. Now the

adjustment can better be checked optical with the mirror cassette. (4822 395 30288). This mirror cassette has no ALP that's why only the influence of the FATG is seen. The right azimuth position is obtained in case the tape moves synchronous over the left and right part of mirror picture. See figure 13 and 14.

On both figures a separate drawing of the mirror picture is shown. On that drawing the head is divided into two equal parts by an imaginary line vertical in the mid of the head surface.
When the tape passes without the ALP guiding there is shown folding line on it. The ideal azimuth position is obtained when both parts of the picture show the same (synchronous) result.

In drawing: the X1 part has to equal to the X2 part. With the Azimuth screw at tape supply side, (left and right from the head, dependant from tape direction, which has to be used) the azimuth can be adjusted.



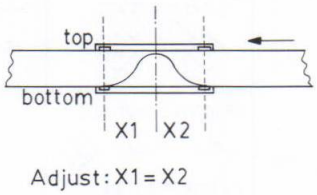
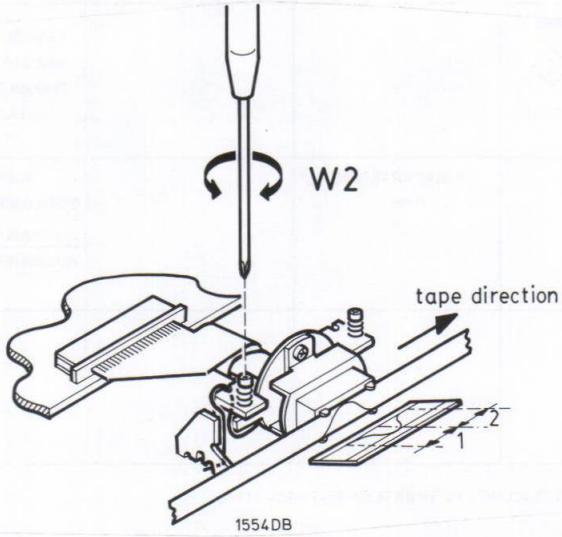


Fig. 13. Azimuth adjustment in Play forward mode.



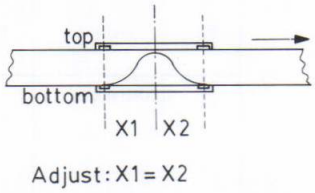


Fig. 14. Azimuth adjustment in Play reverse mode.

ADJUSTMENT TABLE

TOOLS	REMARKS	◇	↻	▭	∿
TAPE SPEED					
USE TEST CASSETTE "SBC420" 3150 Hz 4822 397 30071	PLAYBACK MODE	◇5 OR ◇6 ANAR ANAL	ON TAPE DRIVE PANEL R3543 (A-SIDE) R3542 (B-SIDE)	USE f-COUNTER ADJUST BOTH SIDES TO f = 3150 Hz +/- 0.25 %	
WRITE CURRENT					
USE 9.6 kHz CALIBRATION TAPE 4822 397 30264	PLAYBACK MODE ON READ/WRITE PANEL SHORT CIRCUIT AGC ◇7 ◇10	ON READ/WRITE PANEL ◇2 ◇3 RDSYNC RDMUX			MEASURE PEAK TO PEAK VALUE OF RDMUX SIGNAL TRIGGER ON RDSYNC (AVERAGE VALUE)
	IF RDMUX OUTPUT CLIPS (>3Vpp) CONNECT ◇8 VIA POTMETER OF 47k TO GROUND ◇10		POTMETER 47k		ADJUST UNTIL RDMUX SIGNAL DOESN'T CLIP ANYMORE
USE DCC BLANC CASSETTE	RECORD MODE	◇9 VCLAMP	ON READ/WRITE PANEL R3888		VCLAMP = Iwrite(*) x Rtot ADJUST VCLAMP TO 1.2Vpp(*)
	MAKE RECORDING ON VIRGIN PIECE OF TAPE				
	PLAYBACK MODE PLAYBACK OWN RECORDING	ON READ/WRITE PANEL ◇2 ◇3 RDSYNC RDMUX			MEASURE PEAK TO PEAK VALUE OF RDMUX SIGNAL TRIGGER ON RDSYNC (AVERAGE VALUE)
	RECORD MODE	◇9 VCLAMP	ON READ/WRITE PANEL R3888		ADJUST TO DESIRED WRITE CURRENT = $\frac{\text{Vpp RDMUX 9.6kHz}}{\text{Vpp OWN RECORDING}}$ x 110mA
	REMOVE SHORT CIRCUIT ◇7 ◇10 TO ACTIVATE AGC				

(*) ON FLEXIBLE CABLE OF DCC HEAD, THE ADVISED WRITE CURRENT HAS BEEN INDICATED. VCLAMP = NOTED WRITE CURRENT x Rtot(10 Ohm)

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2.4 Write current adjustment.

In the next an explanation of the write current adjustment as given in the adjustment table of the service manual has been given. The write current has to be adjusted a.o. in case the head support assembly has been replaced.

A. First of all take care that tape speed is within the prescribed tolerances (3150 Hz ± 0.25%).

B. Short circuit the Automatic gain control (AGC) on the read/write board: Interconnect measuring points 7 and 10.

C. Insert the DCC 9.6 kHz level calibration tape (4822 397 30264). With this tape the reference level of the play back mode can be noted. (VppRDMUX)

D. Play back the Calibration level Tape and measure the average peak-peak level of the RDMUX signal on measuring point 3 on R/W board. Trigger oscilloscope on the RDSYNC signal, measuring point 2.

E. In case the RDMUX signal is > 3 Vpp the signal is clipping. Than add a potentiometer of 47kΩ between measuring point 8 and ground (measuring point 10) and adjust with that potentiometer until the RDMUX signal does not clip any more.

F. Insert now a random DCC blanc cassette.

G. Make a recording of a random audio signal.

H. Measure the peak-peak value of the write current between measuring point 9 and ground (measuring point 10). Note this Vclamp value. (Neglect the 4 negative pulses)
This value of Vclamp is defined by:
Vclamp = Iwrite x Rtot.
(Rtot = Resistor value of shunt 3881, 3882, 3883, 3884 = 10Ω)

On the flexible cable of the DCC-head the advised write current in mA has been indicated.
Vclamp should be:
Noted current x Rtot.

Example: Noted current reads: 120
Vclamp is:
120mA x 10Ω = 1.2Vpp

I. Adjust Vclamp to that calculated value under item H by resistor 3888.

In example to 1.2Vpp.

J. Make a recording with this current on a virgin piece of tape.

K. Play back the own recording and measure the average peak-peak level of the RDMUX signal on measuring point 3. Trigger oscilloscope again on the RDSYNC signal, measuring point 2.

L. Calculate the desired write current via next formula:

$$Iwrite = \frac{VppRDMUXoutput9.6kHzleveltape}{VppRDMUXoutputownrecording} x110mA$$

Example: VppRDMUX 9.6 kHz reads: 2.4Vpp
VppRDMUX own recording: 2.3Vpp
Results in desired write current of
114.78 mA, rounded to 115 mA.

M. Put the set in record mode again and adjust the write current with potentiometer 3888 to that calculated value. Measure between measuring point 9 and ground GNDD (measuring point 10)

In the example: Vclamp= Iwrite x Rtot:
Vclamp = 115 mA x 10 = 1.15 Vpp
Adjust with potentiometer 3888 to this value.

N. Do not forget to remove short circuit between measuring point 7 and 10 again, because otherwise the AGC will not operate. In case potentiometer 47kΩ has been added, this additional potentiometer should be removed too.

3 TAPE DRIVE PART ELECTRICAL

The electrical functions of the tape drive part are carried out by:
- Read/Write board
- Digital board
- Tape drive control board

3.1 Read/Write board

The Read/Write board contains the record and playback amplifiers for the DCC head. The recording (write) current is adjustable with one potentiometer. The RDMUX signal is electrical controlled for optimal output level. The ACC playback circuit includes an equalizer (70/120µs circuit) which enables optimal interfacing for the external connected analog circuits like Dolby noise reduction.

The board contains the following functions:
- Read and Write amplifier for DCC head,
- Read amplifier for ACC
- ACC equalizer 70/120µs circuit.

Described in next paragraphs are:
- o the block diagram of the Read/Write board in Write and in Read Mode.
- o Write IC TDA1319T
- o Read IC TDA1317
- o Pin configuration of R/W Connectors
- o Circuit diagram R/W board

The write part done by IC TDA1319T:
- It generates the write pulses for the head.

The read part is done via IC TDA1317:
- Amplifies and multiplexes the head read signals from DCC tapes.
- Amplifies the head signals with ACC playback.

ACC equalization (70/120µsec) is done by separate circuits on the board.

3.1.1 Block diagrams of the Read/Write board

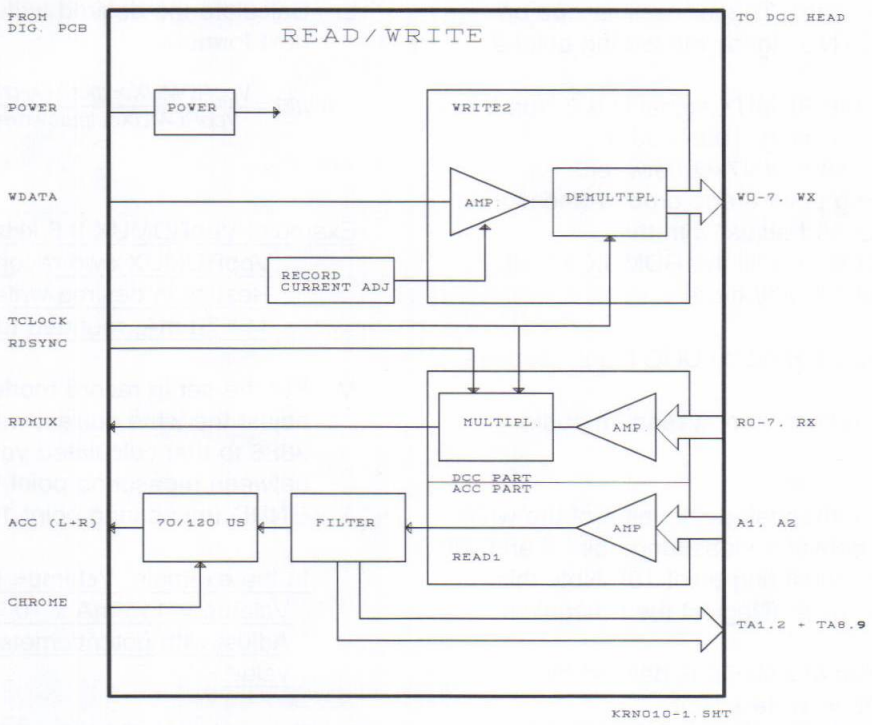

Fig. 15 Block diagram Read/Write board. Write mode

First look to the Write Mode. In figure 15 the block diagram is drawn in Write Mode. The write function is on top of it. The signal flow is from left to right. The input signal WDATA is led to the input amplifiers and via de-multiplexing the serial data are split up into 9 channels, W0 till W7 and WX is the auxiliary channel. The record current can be adjusted via an adjustment of the amplifiers. All signals are clocked via the TCLOCK signal.

The Read Mode is shown on next block diagram, in figure 16. Again the signal flows

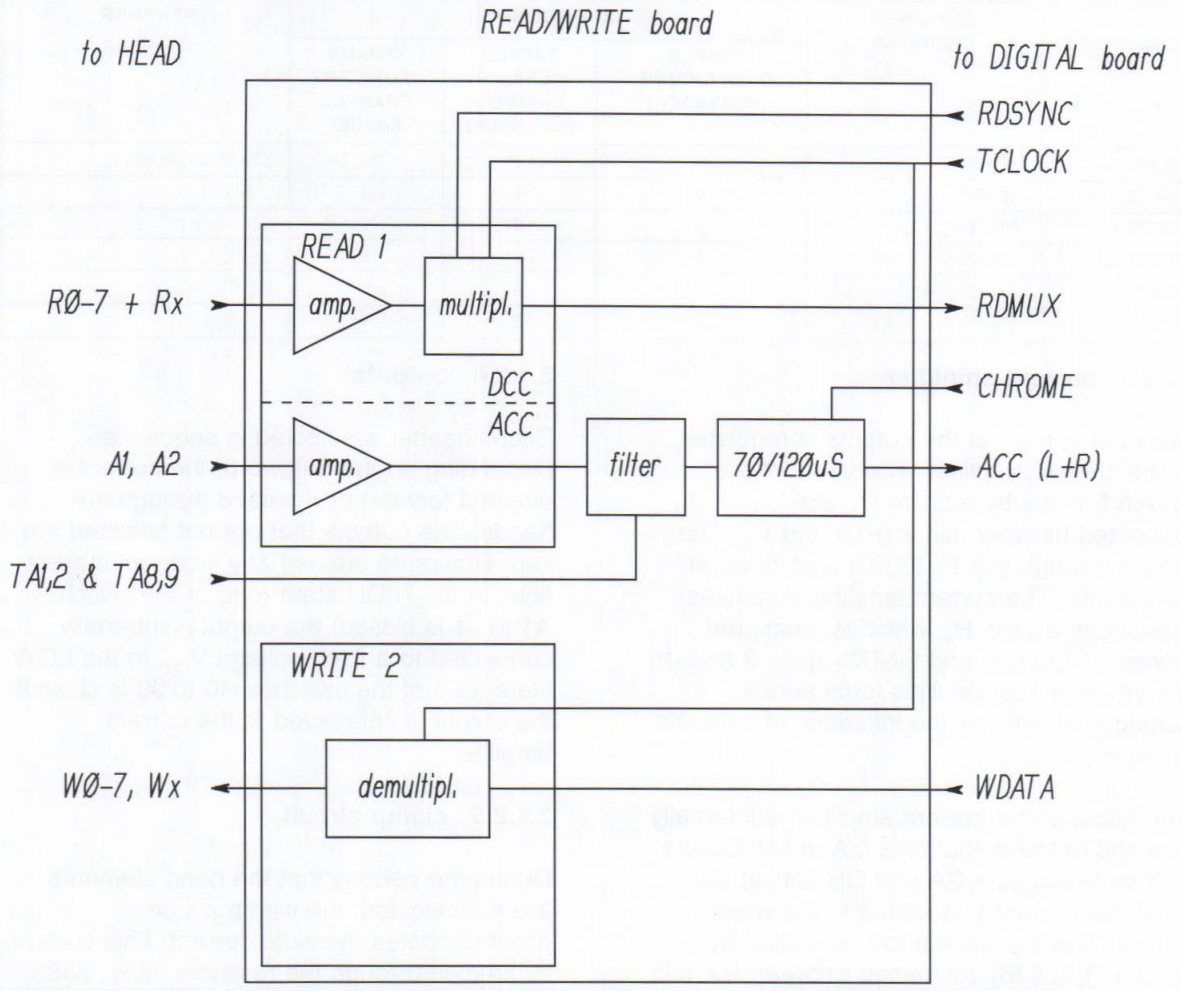

Fig. 16. Block diagram Read/Write board. Read Mode

from left to right and on top of this drawing the Digital read amplifier and the Analog amplifier are drawn.
The by head elements read DCC signal is led to the 9 digital read amplifiers. After multiplexing the RDMUX signal is composed from the 9 digital input channels.
In the next paragraphs the Write and Read ICs are described.

3.1.2 Write IC TDA1319T

The TDA1319T drives the 9 elements of multichannel DCC recording head. The IC forces a current through the selected path. The IC consists of a decoder part, a current amplifier, a Voltage reference, outputs, clamp circuit, standby mode. In figure 17 the contents of the IC is shown in a block diagram.

It contains:
- decoder
- current amplifier
- voltage reference
- outputs
- clamp circuit
- standby mode
- protection

3.1.2.1 decoder part

The DCC write IC is controlled by the 32-bit wide serial dataword which is clocked in at WDATA (pin 12). The clock frequency (WCLK, pin 11) is 3.072 MHz with a clock period of 325 ns. The write pulses are made available at the outputs QA to QJ (pin 13 to 17 and 19 to 23). The dataword also contains control bits, which set the mode of the write amplifier. Control bits TDAPLB, TAUPLB, TERAUX have the following meanings:

DATA CHANNELS 0 TO 7	AUXILIARY CHANNELS	CONTROL BITS[1]			REMARKS
		TDAPLB (DATA CHANNEL PLAYBACK)	TAUPLB (AUXILIARY CHANNEL PLAYBACK)	TERAUX (AUXILIARY CHANNEL ERASE)	
READ	READ	1	1	X	STANDBY MODE
WRITE (I_d)	READ	0	1	X	
WRITE (I_d)	WRITE ($I_d + I_x$)	0	0	0	
WRITE (I_d)	ERASE ($I_d + I_x + I_e$)	0	0	1	
READ	WRITE ($I_d + I_x$)	1	0	0	
READ	ERASE ($I_d + I_x + I_e$)	1	0	1	

3.1.2.2 current amplifier

The write current at the outputs is regulated by the current amplifier. The value of the current I_d is set by resistor R_d 3887, connected between pin 2 (RD) and V_{ss}. The current through this R_d (3387) also flows at the outputs. The current amplifier regulates the voltage across R_d, which is measured between RSENSE and GNDD (pins 3 and 4), to a value of 150mV. This force-sense technique eliminates the influence of parasitic series impedances.

The output of the current amplifier is internally switched to the output pins QA to QJ. During AUX write (outputs QA and QB active) an additional current I_x is added to the write current. This current can be controlled by resistor R_x (3886) connected between RX (pin 1) and GNDD. R_x is chosen to be 6.7 x R_d for achieving 1.2dB current increase.

During the erase mode of the auxiliary channel (TERAUX = HIGH, see above table) it is possible to let an additional output current I_e flow through QA and QB (pins 23 and 22). This extra current (Erase source) can be adjusted with an external resistor R_e (3885) connected between pin 6 and GNDD. Pin 5 (V_{ssE}) is externally connected to ground (GNDD).

3.1.2.3 Voltage reference

A reference voltage is available at pin 9 (REF). This voltage is derived from a bandgap reference source and can be used to modify the voltage sensed by the current amplifier, e.g. for external temperature compensation.

3.1.2.4 outputs

Each channel is selected in sequence. Depending on the dataword, the current is directed forward or reversed through the heads. The outputs that are not selected are kept floating to prevent any incorrect current flow. In the HIGH state (one of the switches A1 to J1 is closed) the output is internally connected to a fixed voltage V_{OH}. In the LOW state (one of the switches A0 to J0 is closed) the output is connected to the current amplifier.

3.1.2.5 clamp circuit

During the periods that the head elements are not selected, the clamp circuit accommodates the write current. This current is directed through the resistors 3881, 3882, 3884 in shunt circuit from pin 24 to the supply. The clamping results in a constant current being drawn from the supply and therefore reduces emission of interferences.

3.1.2.6 standby mode.

The circuit is in the standby mode when TDAPLB = 1 and TAUPLB = 1, or when a HIGH level is applied to pin 10. After a HIGH-to-LOW transition at pin 10, the IC will remain in the standby mode until TDAPLB = 0 or TAUPLB = 0. When the IC is in the standby mode, the current amplifier is switched off to minimize the power consumption, switches A to J are open-circuit and the voltage reference and the erase source are switched off.

3.1.2.7 Protection

The IC is immediately switched to standby mode when a short-circuit to ground at an output pin is detected (V_0 < 0.5V). When the

[1] *X = don't care; 0 = LOW; 1 = HIGH.*

short-circuit condition is removed, the IC will resume operation. The state of the decoder is not affected by a "SHORT".

3.1.2.8 Adjustment

The adjustment of the write current has been described in paragraph 2.4.

3.1.2.9 Block diagram and pin configuration TDA1319T

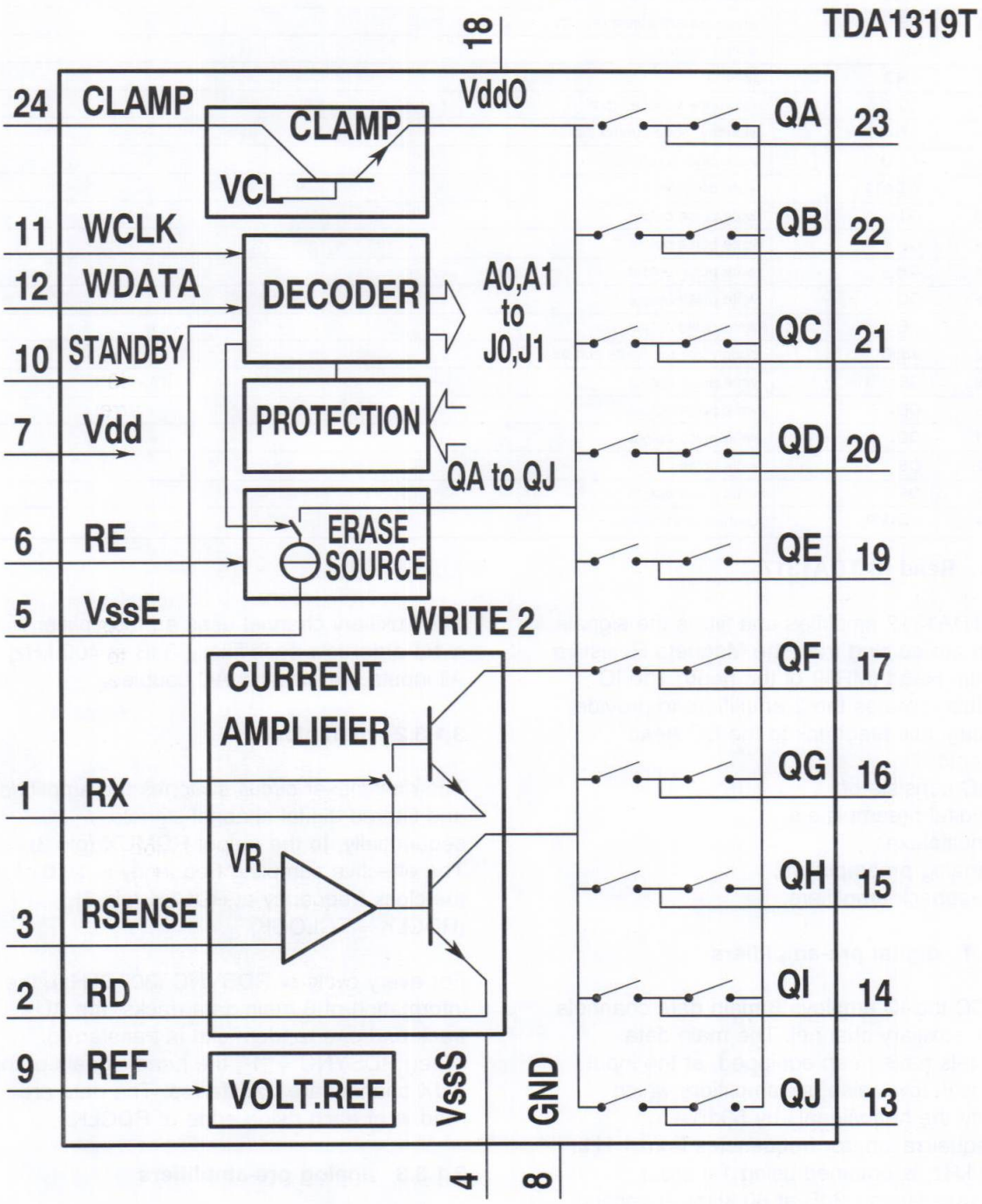

Fig. 17 Write IC TDA1319T

Pin configuration TDA1319T

PIN	NAME	FUNCTION
1	RX	auxiliary current adjust resistor
2	RD	data current adjust resistor
3	RSENSE	sense voltage positive input
4	VssS	sense voltage ground
5	VssE	erase current source ground
6	RE	erase current adjust resistor
7	Vdd	supply voltage
8	GND	ground
9	REF	reference voltage input
10	STANDBY	standby mode control input
11	WCLK	write clock input
12	WDATA	write data input
13	QJ	write pulse output
14	QI	write pulse output
15	QH	write pulse output
16	QG	write pulse output
17	QF	write pulse output
18	VddO	supply voltage (write outputs)
19	QE	write pulse output
20	QD	write pulse output
21	QC	write pulse output
22	QB	write pulse output
23	QA	write pulse output
24	CLAMP	clamp current output

3.1.3 Read IC TDA1317

The TDA1317 amplifies and filters the signals which are coming from the Magneto Resistive thin film Head (MRH) of the head. The IC also incorporates the 2 amplifiers to provide the magnetic feedback to the CC head elements.
The IC consists of:

- digital preamplifiers,
- multiplexer,
- analog preamplifiers,
- feedback amplifiers.

3.1.3.1 digital pre-amplifiers

In DCC the IC employs 8 main data channels and 1 auxiliary channel. The main data channels have been equipped, at the input side, with low-noise pre-amplifiers which amplify the headsignals by 58dB.
Pre-equalization, for frequencies from 1 kHz to 50 kHz, is obtained using 1st order high-pass filters (-3dB at 80 kHz). A second amplifier amplifies, after that filter, the signal by 26 dB. Anti-aliasing of the signal, is achieved by using 2 times 2nd order low-pass filters (-6dB at 135 kHz). See IC block diagram figure 18.

The auxiliary channel uses a preamplifier with a 1st order low-pass filter (-3dB at 400 kHz). All inputs are external AC coupled.

3.1.3.2 multiplexer

The multiplexer circuit switches the amplified and filtered digital channel signals, sequentially, to the output RDMUX (pin 3). The effective sampling frequency is 1/10 of the clock frequency at RDCLK (pin 6). (RDCLK = TCLOCK)

For every cycle of RDSYNC (307,2kHz), the information of 8 main data tracks, the AUX track and one random slot is transferred. When RDSYNC = "1", the head signals of the AUX channel are transferred. The data are read in at each rising edge of RDCLK.

3.1.3.3 analog pre-amplifiers

In case an ACC cassette is inserted the ACC playback signal is read. The 2 low-noise preamplifiers raise the 2 analog track signals by 44 dB. Also the analog input is AC coupled.

3.1.3.4 feedback amplifier.

Two feedback amplifiers are provided for driving a coil in the MRH (magnetic resistor head). This amplifier provides a feedback loop in order to improve the linearity of the frequency response of the analog audio signal. Together with the bias-signal of the Barkhausen noise suppression generator on the Read/Write board, the Barkhausen noise from the tape, is suppressed too.

3.1.3.5 Block diagram and pin configuration TDA1317.

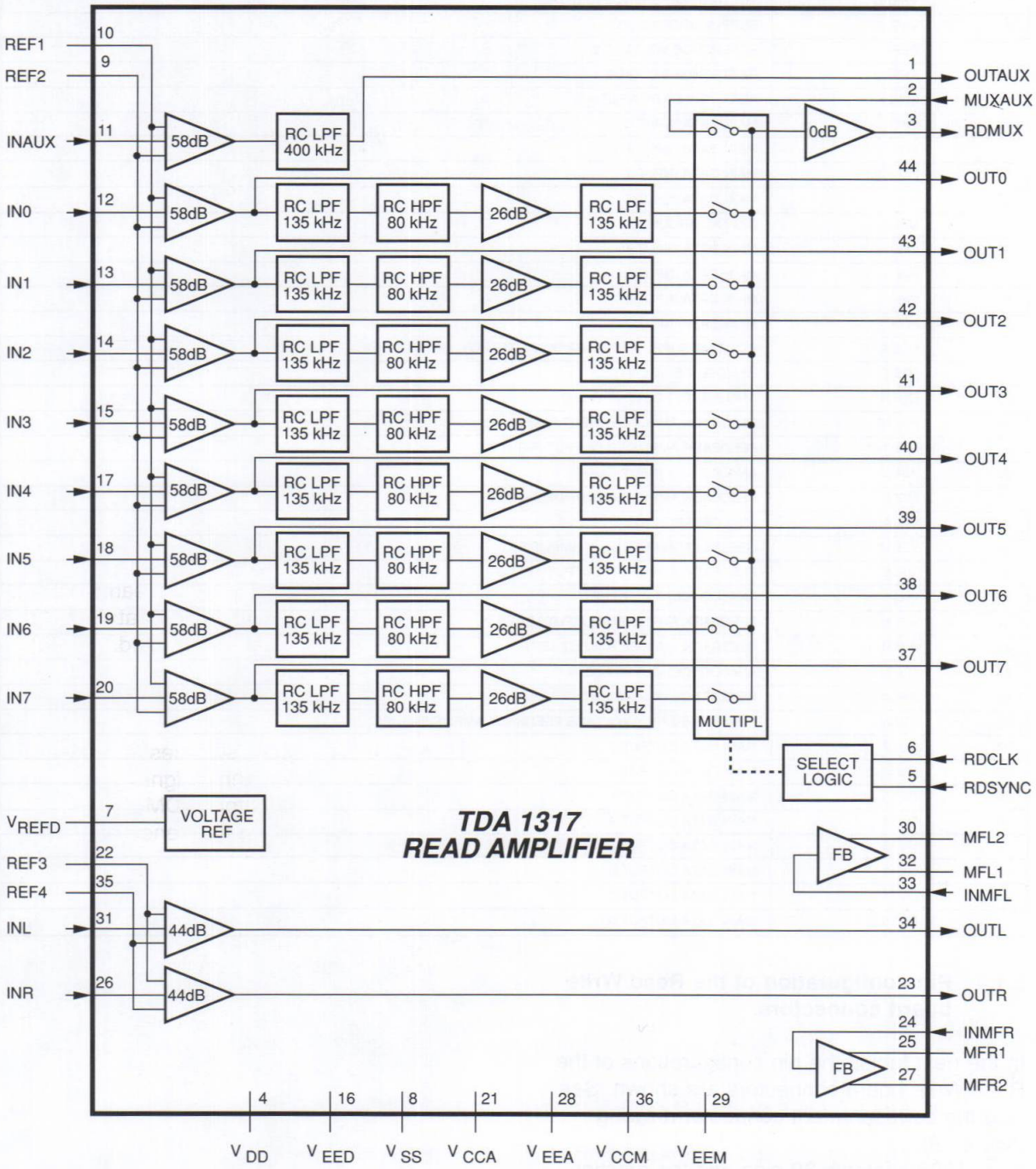

Fig. 18 Read amplifier IC TDA1317 and pin configuration

Pin configuration TDA1317

PIN	NAME	FUNCTION
1	OUTAUX	AUXILIARY DATA OUTPUT
2	MUXAUX	AUXILIARY MULTIPLEXER INPUT
3	RDMUX	READ MULTIPLEXER OUTPUT
4	VDD	POSITIVE SUPPLY VOLTAGE DCC-PART (+5V)
5	RDSYNC	READ SYNC INPUT
6	RDCLK	READ CLOCK INPUT
7	VREFD	VOLTAGE REFERENCE (DIGITAL)
8	VSS	SUPPLY GROUND (0V)
9	REF2	REFERENCE VOLTAGE 2
10	REF1	REFERENCE VOLTAGE 1
11	INAUX	AUXILIARY DATA INPUT
12	IN0	MAIN DATA INPUT 0
13	IN1	MAIN DATA INPUT 1
14	IN2	MAIN DATA INPUT 2
15	IN3	MAIN DATA INPUT 3
16	VEED	DIGITAL GROUND
17	IN4	MAIN DATA INPUT 4
18	IN5	MAIN DATA INPUT 5
19	IN6	MAIN DATA INPUT 6
20	IN7	MAIN DATA INPUT 7
21	VCCA	POSITIVE SUPPLY VOLTAGE CC-PART (+5V)
22	REF3	REFERENCE VOLTAGE 3
23	OUTR	ANALOG (CC) OUTPUT RIGHT
24	INMFR	FEEDBACK AMPLIFIER INPUT RIGHT
25	MFR1	FEEDBACK AMPLIFIER OUTPUT RIGHT 1
26	INR	ANALOG (CC) INPUT RIGHT
27	MFR2	FEEDBACK AMPLIFIER OUTPUT RIGHT 2
28	VEEA	ANALOG GROUND
29	VEEM	GROUND FOR FEEDBACK AMPLIFIER
30	MFL2	FEEDBACK AMPLIFIER OUTPUT LEFT 2
31	INL	ANALOG (CC) INPUT LEFT
32	MFL1	FEEDBACK AMPLIFIER OUTPUT LEFT 1
33	INMFL	FEEDBACK AMPLIFIER INPUT LEFT
34	OUTL	ANALOG (CC) OUTPUT LEFT
35	REF4	REFERENCE VOLTAGE 4
36	VCCM	POSITIVE SUPPLY VOLTAGE FEEDBACK AMPLIFIER (+5V)
37	OUT7	MAIN DATA OUTPUT 7
38	OUT6	MAIN DATA OUTPUT 6
39	OUT5	MAIN DATA OUTPUT 5
40	OUT4	MAIN DATA OUTPUT 4
41	OUT3	MAIN DATA OUTPUT 3
42	OUT2	MAIN DATA OUTPUT 2
43	OUT1	MAIN DATA OUTPUT 1
44	OUT0	MAIN DATA OUTPUT 0

3.1.4 Pin configuration of the Read/Write board connectors.

In the next tables the pin configurations of the Read/Write board connectors are shown. See also the correspondent connector drawing (figure 19).
Item 1800 contents 30 pins and the function is DCC head interface.
Item 1801 contents 18 pins and its function is Digital board interface

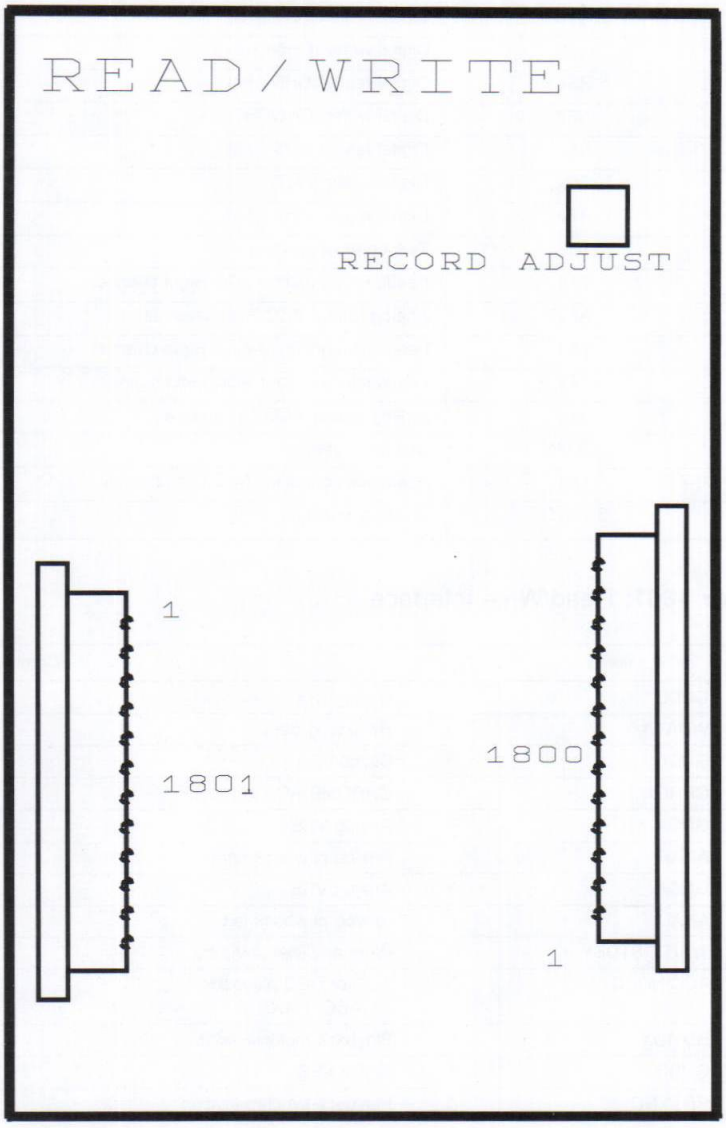

Fig. 19 Read/Write board connectors

Connector 1800: DCC-Head interface

Pin No.	Name	Comment
1	TD1	Test conductor digital
2	WX-	Digital writer (AUX channel)
3	RX+	Digital reader AUX channel (Hot)
4	WX0	Digital writer (AUX channel/CH0)
5	R0+	Digital reader CH0 (Hot)
6	W01	Digital writer (CH0/CH1)
7	R1+	Digital reader CH1 (Hot)
8	W12	Digital writer (CH1/CH2)
9	R2+	Digital reader CH2 (Hot)
10	W23	Digital writer (CH2/CH3)
11	R3+	Digital reader CH3 (Hot)
12	W34	Digital writer (CH3/CH4)
13	COD	Common digital

14	W45	Digital writer (CH4/CH5)
15	R4+	Digital reader CH4 (Hot)
16	W56	Digital writer (CH5/CH6)
17	R5+	Digital reader CH5 (Hot)
18	W67	Digital writer (CH6/CH7)
19	R6+	Digital reader CH6 (Hot)
20	W7-	Digital writer (CH7)
21	R7+	Digital reader CH7 (Hot)
22	TD2	Test conductor digital
23	TA8	Feedback conductor ACC Right channel
24	A2+	Analog reader ACC Right channel
25	TA9	Feedback conductor ACC Right channel
26	TA1	Feedback conductor ACC Left channel
27	A1+	Analog reader ACC Left channel
28	COA	Common analog
29	TA2	Feedback conductor ACC Left channel
30	SHIELD	Shield connection

Connector 1801: Read/Write interface

Pin No.	Name	Type[2]	Comment
1	GNDD	P	Digital VSS
2	WDATA	O	Recording data
3	GNDD	P	Digital VSS
4	CHROME	O	CHROME ACC indication
5	GNDA	P	Analog VSS
6	ANAR	I	Analog playback right
7	GNDA	P	Analog VSS
8	ANAL	I	Analog playback left
9	WRITE-STDBY	O	Write amplifier stand-by
10	ACC/NDCC	O	ACC or DCC playback (H=ACC, L=DCC)
11	RDMUX	I	Playback multiplexed data
12	GNDD	P	Digital VSS
13	RDSYNC	O	Playback synchronization
14	GNDD	P	Digital VSS
15	TCLOCK	O	Playback/record clock
16	GNDD	P	Digital VSS
17	+5VD	P	5 Volt digital supply output
18	+10VD	P	10 Volt digital supply output

3.1.5 Circuit diagram of the Read/Write board.

In next figure 20 the circuit diagram of the Read/Write board has been drawn. Mark the displayed signals of TCLOCK, RDSYNC, RDMUX and WDATA.

[2]*Note: P= Power; I= Input, aI= Analog Input; O= Output; aO= Analog Output; I/O= Input/Output*

33 CIRCUIT DESCRIPTION

33 CIRCUIT DESCRIPTION

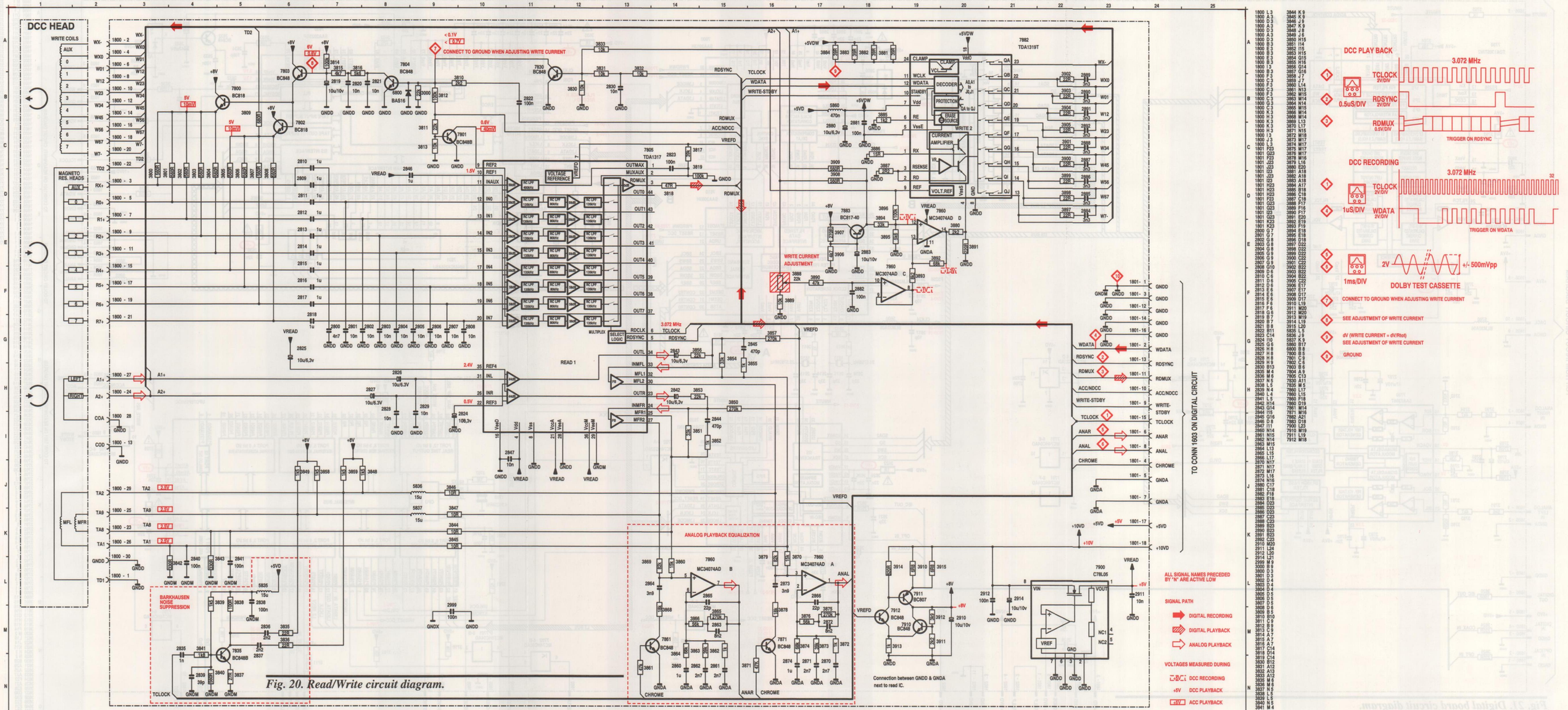

Fig. 20. Read/Write circuit diagram.

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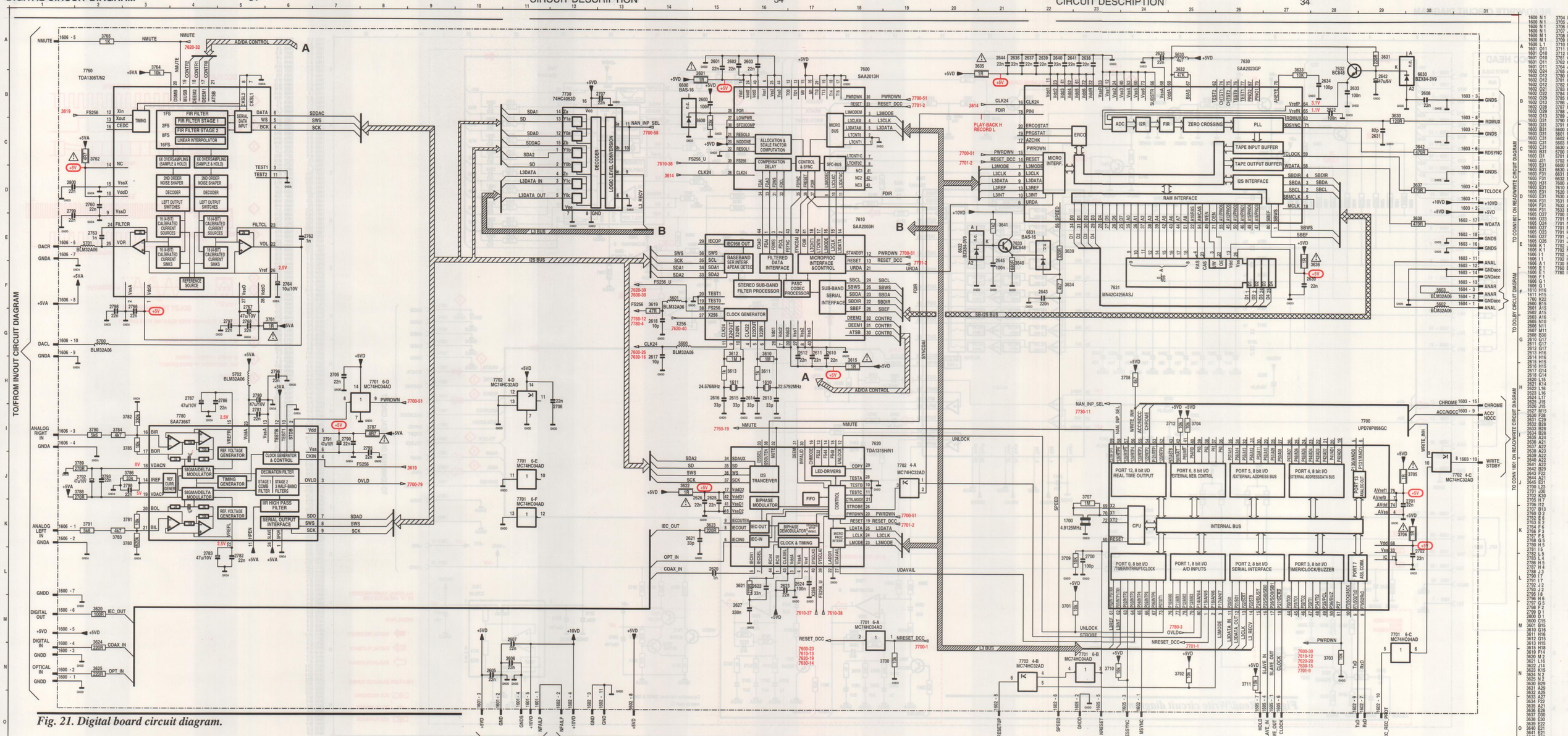

Fig. 21. Digital board circuit diagram.

3.2 Digital board

3.2.1 Block diagram

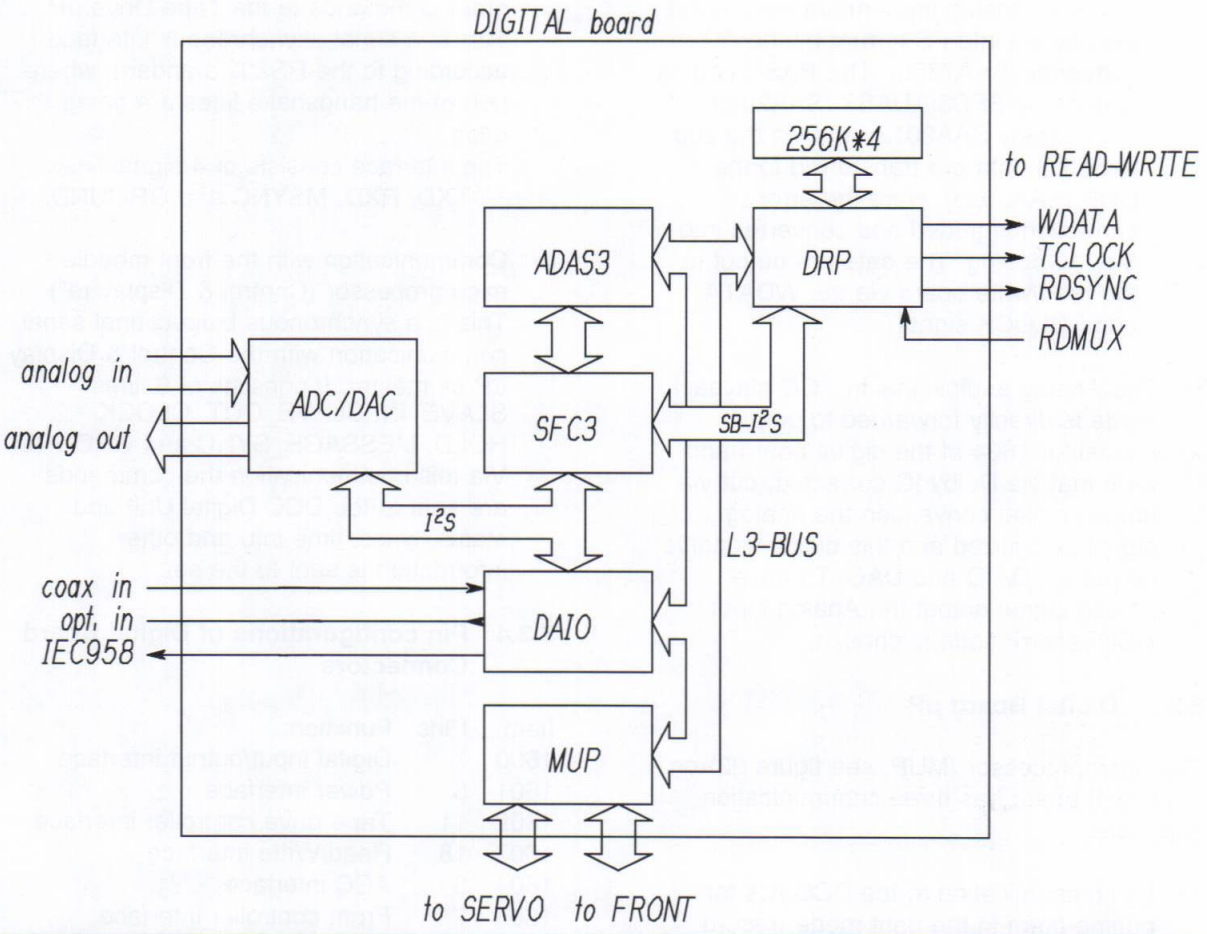

Fig. 22. Block diagram Digital board of the DCC Deck Unit

The block diagram is explained in the following paragraphs:

- Operation modes of the Digital Board
- Digital Board µP
- Pin configuration of Digital Board connectors
- VLSI of Digital Board
- Digital Board circuit diagram

3.2.2 Operation modes of the Digital Board

From all four operating modes in the DCC recorder the digital board takes care of them (see also circuit diagram figure 21):

- Data playback, Aux playback
- Data record, Aux record
- Data playback, Aux record
- ACC Playback

These 4 modes are already described in detail at chapter 1.3 Block diagram DCC951, see paragraph 1.3.1. Operation modes.

Next a summery of the activities on the digital board in DCC-playback and DCC-record mode is described.

- DCC-playback:
  In this mode the RDMUX signal coming from the read/write board is de-multiplexed and decoded by the DRP (SAA2023) and transferred to the SFC3 (SAA2003) via the SB-I²S. In the SFC3 the PASC decoding is performed and the audio data are output in I²S format. Via the DAIO (TDA1315) the audio data are available in IEC958 format (digital out). The DAC IC is TDA1305.

- DCC-record:
  The source can be analog or digital. With a digital source the IEC958 input signal is transferred in DAIO (TDA1315) to I^2S. In analog input mode the input is transferred into I^2S format by the AD convertor (SAA7366). The PASC coding is done by SFC3/ADAS3 (SAA2003 respectively SAA2013) and via the sub band I^2S data are transferred to the DRP (SAA2023). Here the error correction is added and converted into 8-to-10 coding. The data are output to the read/write board via the WDATA and TCLOCK signal.

- The Analog audiosignal in ACC playback mode is directly forwarded to output connector 1604 of the digital board and after that via Dolby IC corrected, but via analog digital conversion the analog signal is digitized and this digital signal is output via DAIO and DAC. To have analog signal output the Analog input DCC-record mode is chosen.

3.2.3 Digital Board μP

The microprocessor (MUP, see figure 22) on the digital board has three communication channels:

1• L3 communication to the DCC ICs for putting them in the right mode (record, playback, analog input etc) and reading the sub code and other information from the DCC ICs.

2• Communication with the Tape Drive μP of the tape drive board for reading the status of the switches on the deck/loader and for sending wind, rewind, play and other commands to the Tape Drive μP. This is a serial asynchronous interface according to the RS232 standard, where non of the handshake lines are being used.
The interface consists of 4 signal lines:
TXD, RXD, MSYNC and GROUND.

3• Communication with the front module microprocessor (Control & Display μP). This is a synchronous bidirectional serial communication with the Control & Display μP as master. It consists of 6 lines: SLAVE_IN, SLAVE_OUT, CLOCK, HOLD, MESSAGE_SYNC and GROUND. Via this communication the commands are sent to the DCC Digital Unit and status, lyrics, time info and other information is sent to the set.

3.2.4 Pin configurations of Digital Board Connectors

Item:	Pins:	Function:
1600	7	Digital input/output interface
1601	5	Power interface
1602	11	Tape drive controller interface
1603	18	Read/Write interface
1604	3	ACC interface
1605	7	Front controller interface
1606	10	Analog input/output interface

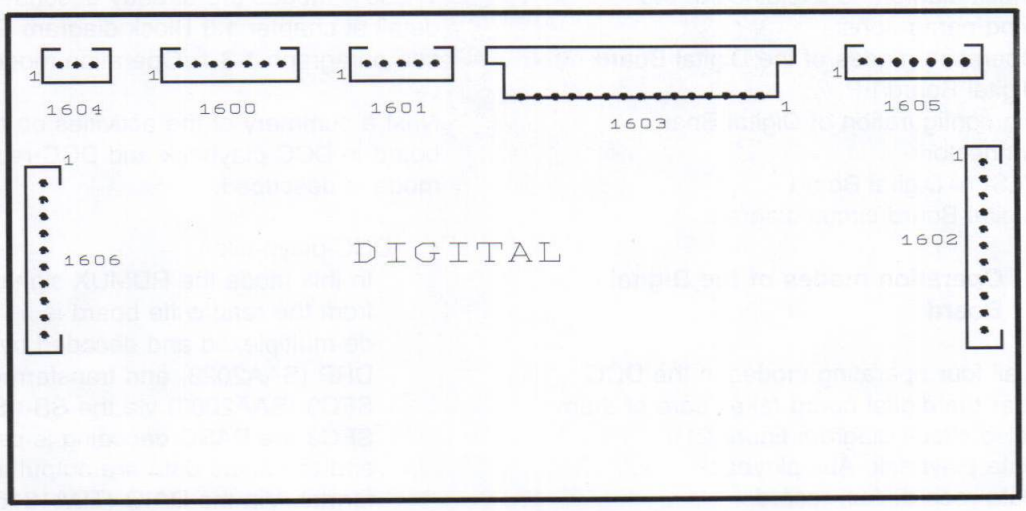

Fig. 23 Digital Board connectors

Connector 1600: Digital input/output interface

Pin No.	Name	Type[3]	Comment
1	GNDD	P	Digital ground
2	OPTICAL IN	I	IEC958 input from optical receiver
3	GNDD	P	Digital ground
4	COAXIAL IN	I	IEC958 high sensitive input
5	+5VD	P	+5VD supply output for optical receiver/transmitter
6	DIGITAL OUT	O	IEC958 output
7	GNDD	P	Digital ground

Connector 1601: Power interface

Pin No.	Name	Type	Comment
1	N_FAILP	I	Mains power fail indication (L = power failure)
2	GNDD	P	Digital ground
3	+5VD	P	Digital 5 Volt supply input
4	GNDS	P	Analog motors ground
5	+10VD	P	Digital 10 Volt supply input

Connector 1602: Tape Drive Controller interface

Pin No.	Name	Type	Comment
11	GNDD	P	Digital VSS
10	NDCC-REC-PROT	I	DCC record protection switch input
9	TXD	O	Serial data output to tape drive unit
8	+5VD	P	+5 Volt digital supply output
7	RXD	I	Serial data input from tape drive unit
6	SPEED	O	Analog control signal for capstan control
5	RESET_UP	O	Reset tape drive board μP
4	+10VD	P	10 volt digital supply output
3	GNDS	P	Analog motors ground
2	N_FAILP	O	Mains power fail indication to tape drive board (L = power failure)
1	MSYNC	I/O	Message synchronisation with Digital μP, indication line of block transfers.

Connector 1603: Read/Write interface

Pin No.	Name	Type	Comment
18	GNDD	P	Digital VSS
17	WDATA	O	Recording data
16	GNDD	P	Digital VSS
15	CHROME	O	CHROME ACC indication
14	GNDA	P	Analog VSS
13	ANAR	I	Analog playback right
12	GNDA	P	Analog VSS
11	ANAL	I	Analog playback left
10	WRITE-STDBY	O	Write amplifier stand-by
9	ACC/NDCC	O	ACC or DCC playback (H=ACC, L=DCC)
8	RDMUX	I	Playback multiplexed data
7	GNDD	P	Digital VSS
6	RDSYNC	O	Playback synchronization
5	GNDD	P	Digital VSS
4	TCLOCK	O	Playback/record clock
3	GNDD	P	Digital VSS
2	+5VD	P	5 Volt digital supply input
1	+10VD	P	10 Volt digital supply input

[3]*Note: P= Power; I= Input, aI= Analog Input; O= Output; aO= Analog Output; I/O= Input/Output*

Connector 1604: ACC interface

Pin No.	Name	Type	Comment
1	ACCL	aO	ACC output Left
2	GNDA	P	Analog ground
3	ACCR	aO	ACC output Right

Connector 1605: Front controller interface

Pin No.	Name	Type	Comment
1	SLAVE_OUT	O	Serial data **to** user controller
2	GNDD	P	Digital Ground
3	MESSYNC	I/O	Message synchronization with user controller
4	SLAVE_IN	I	Serial data **from** user controller
5	NRESET	I	Master reset Digital Unit (L=reset)
6	CLOCK	I	Serial data clock from controller
7	HOLD	O	DDU is busy flag

Connector 1606: Analog input/output interface

Pin No.	Name	Type	Comment
1	LEFT INPUT	aI	Analog audio input left
2	GNDA	P	Analog ground
3	RIGHT INPUT	aI	Analog audio input right
4	GNDA	P	Analog ground
5	NMUTE	O	Mute for audio channels (active low)
6	DACR	aO	Analog audio output right
7	GNDA	P	Analog ground
8	+5VA	P	+5 Volt analog supply input
9	GNDA	P	Analog ground
10	DACL	aO	Analog audio output left

3.2.5 DCC ICs on Digital Board

In the next figures and tables the block diagrams and pin configurations of the typical DCC ICs are shown in the next following order:

DRP	SAA2023
SFC3	SAA2003
ADAS3	SAA2013
DAIO	TDA1315
DAC	TDA1305
ADC	SAA7366.

3.2.5.1 Digital Equalizer & Tape Formatting and Error coding unit(DRP) IC SAA2023

IC SAA2023 performs the drive processor function in the DCC system. This IC is built up of digital equalizer, error correction and tape formatting functions. The DCC drive processing concerns the following functions:

In Play back mode:

- Analog-to-digital conversion of the head signals.
- Tape channel equalization,
- Tape channel data and clock recovery,
- 10-to-8 demodulation
- Data placement in system RAM
- C1 and C2 errror correction decoding
- Interfacing to sub-band serial PASC interface
- Interfacing to Main μP for SYSINFO and AUX data
- Capstan speed control for tape deck.

In Record mode:

- Interfacing to sub-band serial PASC interface
- C1 and C2 error correction encoding
- Formatting for tape transfer
- 8-to-10 modulation
- Interfacing to Main μP for SYSINFO and AUX data
- Capstan speed control for tape deck, programmed by tape drive board μP

In Search mode:

- Detection and interpretation of AUX envelope information
- AUX envelope counting
- Search speed estimation

So the DRP takes care for the control of capstan speed during DCC-recording and DCC-playback too.

In Search mode the tape speed is measured and the envelope information of the AUX signal is detected and interpreted.
The IC also offers Digital and Analogue Eyepattern outputs of the incoming signal from the head. This application is used in the Service test mode.

In Play mode the DCC Drive Processor (DRP) reconstructs the original digital head signals, and after digital equalizing and Error correction procedures, together with DRAM IC MN4C4256, the digital data are recovered and demodulated from 10-to-8 bits. Via the sub-band interface all signals are formatted to the subband serial PASC data bus. This 'SB-I^{2}S-Bus' forwards the signal to the SFC3 (SAA2003). Sub-code information (Sub-code = System information + Auxiliary information) goes to the Main µP via the L3-Bus.

In Data record, Aux record mode, the PASC frames of data are now via 'SBI^{2}S-Bus' sent from SFC3 to the DRP.
In the DRP the subband samples are received in the subband serial PASC interface.
In the recording mode Tape Formatting and Error correction (TFE) part of this IC, the C1 and C2 error corrections are encoded and the signal is formatted for tape transfer.
The tape frame data are passed on serially to the write amplifier.

In Data playback, Aux record mode the AUX envelope is written anew on track. The DRP continuously sends sub-code data to the Main µP, and simultaneously generates AUX tape frames. The tape frames generated by the DRP are taken in serial form via WDATA to the write amplifier.

BLOCK DIAGRAM AND PIN CONFIGURATION SAA2023.

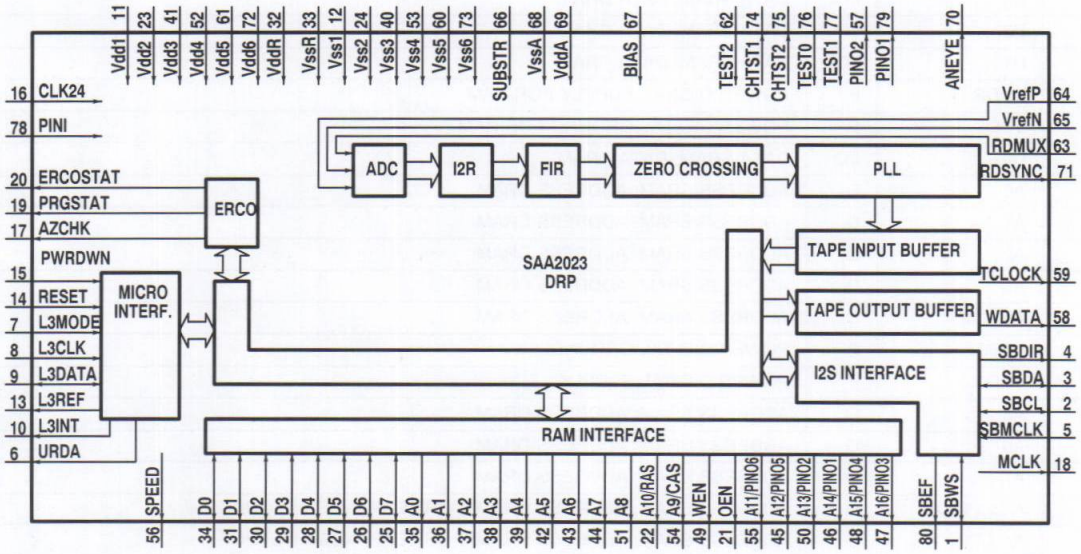

Fig. 24. SAA2023: Drive processor (DRP)

PIN CONFIGURATION SAA2023

PIN	NAME	I/O	FUNCTION
1	SBWS	I/O	WORD SELECTOR FOR SB -I²S INTERFACE
2	SBCL	I/O	BIT CLOCK FOR SB-I²S INTERFACE
3	SBDA	I/O	DATA LINE FOR SB-I²S INTERFACE
4	SBDIR	O	DIRECTION LINE FOR SB-I²S INTERFACE
5	SBMCLK	I	MASTER CLOCK FOR SB-I²S INTERFACE
6	URDA	O	UNRELIABLE DATA
7	L3MODE	I	MODE LINE FOR L3 INTERFACE
8	L3CLK	I	BIT CLOCK LINE FOR L3 INTERFACE
9	L3DATA	I/O	SERIAL DATA LINE FOR L3 INTERFACE
10	L3INT	O	L3 INTERRUPT OUTPUT
11	VDD1	P	DIGITAL POSITIVE SUPPLY
12	VSS1	P	DIGITAL GROUND
13	L3REF	O	L3 BUS TIMING REFERENCE
14	RESET	I	RESET DRP CHIP
15	PWRDWN	I	PUT DRP INTO POWER DOWN MODE
16	CLK24	I	24.576 MHZ CLOCK INPUT
17	AZCHK	O	CHANNEL 0 AND CHANNEL 7 AZIMUTH MONITOR
18	MCLK	O	6.144 MHZ CLOCK OUTPUT
19	PRGSTAT	O	TFE3 PROGRAM STATUS, FOR TEST ONLY
20	ERCOSTAT	O	ERCO STATUS, FOR TEST ONLY
21	OEN	O	OUTPUT ENABLE FOR RAM
22	A 1 0/RAS	O	ADDRESS SRAM; RAS DRAM
23	VDD2	P	POWER DIGITAL SUPPLY
24	VSS2	P	POWER DIGITAL GROUND
25	D7	I/O	DATA SRAM;
26	D6	I/O	DATA SRAM;
27	D5	I/O	DATA SRAM;
28	D4	I/O	DATA SRAM;
29	D3	I/O	DATA SRAM; DATA DRAM
30	D2	I/O	DATA SRAM; DATA DRAM
31	D1	I/O	DATA SRAM; DATA DRAM
32	VDDR	P	POWER DIGITAL SUPPLY FOR RAM
33	VDDS	P	POWER DIGITAL GROUND FOR RAM
34	D0	I/O	DATA SRAM; DATA DRAM
35	A0	O	ADDRESS SRAM; ADDRESS DRAM
36	A1	O	ADDRESS SRAM; ADDRESS DRAM
37	A2	O	ADDRESS SRAM; ADDRESS DRAM
38	A3	O	ADDRESS SRAM; ADDRESS DRAM
39	A4	O	ADDRESS SRAM; ADDRESS DRAM
40	VSS3	P	POWER DIGITAL GROUND
41	VDD3	P	POWER DIGITAL SUPPLY
42	A5	O	ADDRESS SRAM; ADDRESS DRAM
43	A6	O	ADDRESS SRAM; ADDRESS DRAM
44	A7	O	ADDRESS SRAM; ADDRESS DRAM
45	A1 2/PINO5	O	ADDRESS SRAM; ADDRESS DRAM; PORT EXPANDER OUTPUT 5
46	A1 4/PINO1	O	ADDRESS SRAM; ADDRESS DRAM; PORT EXPANDER OUTPUT 1
47	A1 6/PINO3	O	ADDRESS SRAM; ADDRESS DRAM; PORT EXPANDER OUTPUT 3
48	A1 5/PINO4	O	ADDRESS SRAM; ADDRESS DRAM; PORT EXPANDER OUTPUT 4
49	WEN	O	WRITE ENABLE FOR RAM
50	A1 3/PINO2	O	ADDRESS SRAM; ADDRESS DRAM; PORT EXPANDER OUTPUT 2
51	A8	O	ADDRESS SRAM; ADDRESS DRAM
52	VDD4	P	POWER DIGITAL SUPPLY
53	VSS4	P	POWER DIGITAL GROUND
54	A9/CAS	O	ADDRESS SRAM; CAS FOR DRAM
55	A11	O	ADDRESS SRAM
56	SPEED	TO	PWM CAPSTAN CONTROL OUTPUT FOR DECK

57	PINO2/SPEE-DB	TO	PORT EXPANDER OUTPUT 2/ PWM CAPSTAN CONTROL OUTPUT FOR DECK B
58	WDATA	O	SERIAL OUTPUT TO WRITE AMPLIFIER
59	TCLOCK	O	3.072 MHZ CLOCK OUTPUT FOR TAPE I/O
60	VSS5	P	POWER DIGITAL GROUND
61	VDD5	P	POWER DIGITAL SUPPLY
62	TEST2	ID	TEST MODE SELECT
63	RDMUX	IA	ANALOGUE MULTIPLEXED INPUT FROM READ AMPLIFIER
64	VREFP	IA	ADC REFERENCE VOLTAGE P
65	VREFN	IA	ADC REFERENCE VOLTAGE N
66	SUBSTR	IA	SUBSTRATE CONNECTION
67	BIAS	IA	BIAS CURRENT FOR ADC
68	VSSA	P	ANALOGUE GROUND
69	VDDA	P	ANALOGUE SUPPLY
70	ANAEYE	OA	ANALOGUE EYE PATTERN OUTPUT
71	RDSYNC	O	SYNCHRONISATION OUTPUT FOR READ AMPLIFIER
72	VDD6	P	POWER DIGITAL SUPPLY
73	VSS6	P	POWER DIGITAL GROUND
74	CHTST1	O	CHANNEL TEST PIN 1
75	CHTST2	O	CHANNEL TEST PIN É
76	TEST0	ID	TEST MODE SELECT
77	TEST1	ID	TEST MODE SELECT
78	PINI	I	PORT EXPANDER INPUT
79	PINO1	O	PORT EXPANDER OUTPUT 1
80	SBEF	O	SB-I²S ERROR FLAG LINE

3.2.5.2 Sub-band filter and PASC encoder/decoder(SFC3) IC SAA2003

IC SAA2003 performs the sub-band filtering and audio frame codec functions in the PASC System.
In Play back mode the IC receives the sub-band serial PASC data via the 'SB-I²S-Bus'. These are the signal lines: SBWS, SBCL, SBDA, SBDIR, SBEF. The Stereo Filter and Codec IC recovers the frames of data from the DRP. The PASC decoded sub-band samples are reconstructed by the sub-band filters into a single complete digital audio signal (SD2).
Sub-code information (Sub-code = System information + Auxiliary information) come to the Main µP via the L3-Bus. Signal lines are:
LTCNTO,
LTNCT1, L3DATA, L3CLK, L3MODE, FDIR, SYNCDAI, SLEEP, RESET, URDA.

In Data record, Aux record mode the digital audio data are fed via I²S bus (WS, SCK, SD1) to SFC3. Here, the broadband signal is separated into 32 sub-bands for left and right channels and a PASC frame is generated.
In the ADAS a complete frame of subband data is collected before the allocation and scale factor information can be calculated. To have that information available in the same time frame as the audio samples are at the output, the subband filtered samples in the Stereo Filter and Codec IC (SFC3) are delayed. (Dependant to the audio sample rate of 32, 44.1 or 48 kHz.) The delayed samples are passed to the codec part of SFC3 on the filtered data interface bus, (FSYNC, FDCL, FDWS, FDAO, FDAI signal lines), on the FDAO pin.
Synchronization, allocation and scale factor are added in SFC3 to provide a fully PASC data signal. These frames of data are now via 'SBI²S-Bus' sent to the DRP.

BLOCK DIAGRAM

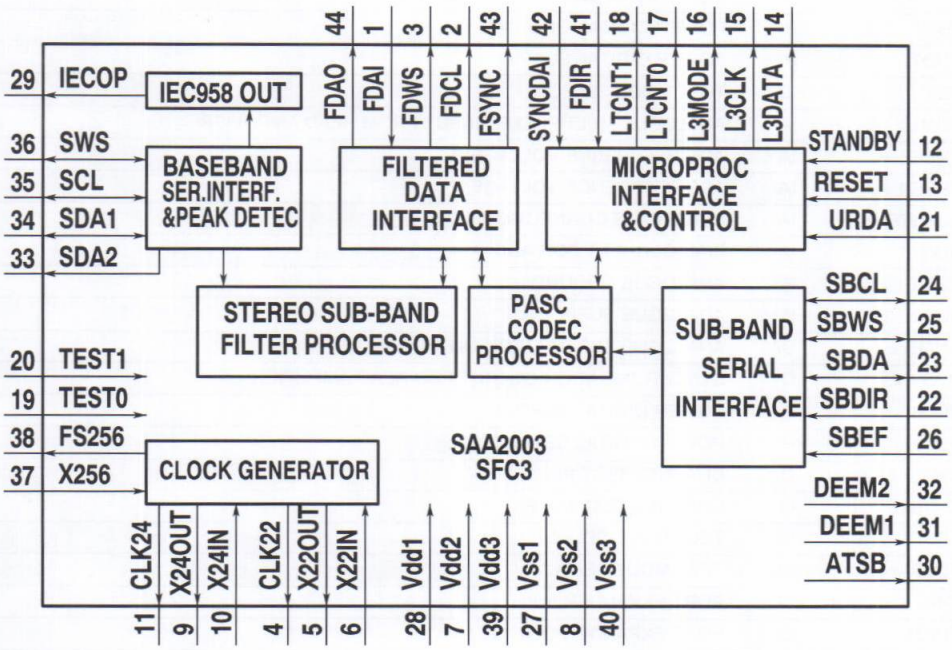

Fig. 25. SAA2003: Sub-band filter (SFC3)

PIN CONFIGURATION SAA2003

PIN	NAME	I/O	FUNCTION
1	FDAI	I	filtered serial data input(from ADAS)
2	FDCL	O	filtered data bit clock
3	FDWS	O	filtered data word select
4	CLK22	O	22.5792 MHz buffered clock output
5	X22OUT	O	22.5792 MHz XTAL oscillator output
6	X22IN	I	22.5792 MHz XTAL oscillator input
7	VDD2	P	positive supply(clock oscillators)
8	VSS2	P	supply ground(clock oscillators)
9	X24OUT	O	24.576 MHz XTAL oscillator output
10	X24IN	I	24.576 MHz XTAL oscillator input
11	CLK24	O	24.576 MHz XTAL buffered clock output
12	STANDBY	I	device inactive
13	RESET	I	device reset
14	L3DATA	I/O	L3 interface serial data
15	L3CLK	I	L3 interface bit clock
16	L3MODE	I	L3 interface mode control
17	LTCNT0	I	LT compatible interface mode control
18	LTCNT1	I	LT compatible interface mode control
19	TEST0	I	test mode select
20	TEST1	I	test mode select
21	URDA	I	unreliable data from drive processing
22	SBDIR	I	sub-band data direction
23	SBDA	I/O	sub-band serial data
24	SBCL	I/O	sub-band bit clock
25	SBWS	I/O	sub-band word select

26	SBEF	I	sub-band error flag from drive processing
27	VSS1	P	supply ground(logic)
28	VDD1	P	positive supply(logic)
29	IECOP	O	IEC958 digital audio output
30	DEEMDAC	O	DAC control or general purpose output
31	ATTDAC	0	DAC control or general purpose output
32	MUTEDAC	O	DAC control or general purpose output
33	SDA2	O	baseband serial data output to DAC
34	SDA1	I/O	baseband serial data to/from DAIO and ADC
35	SCL	I/O	baseband bit clock
36	SWS	I/O	baseband word select
37	X256	I	master audio clock input from external source
38	FS256	O	master audio clock at 256x sample frequency
39	VDD3	P	positive supply(FS256 pin)
40	VSS3	P	supply ground(FS256 pin)
41	FDIR	O	PASC mode encode/decode
42	SYNCDAI	O	settings synchronisation for DAIO
43	FSYNC	O	sub-band 0 sample synchronisation
44	FDAO	O	filtered serial data output(to ADAS)

3.2.5.3 Adaptive Allocation and Scalefactor processor(ADAS3) IC SAA2013

The IC SAA2013 performs the Adaptive Allocation and Scaling functions in the Precision Adaptive Sub-band Coding (PASC) system. It is only used during recording together with Stereo Filter and Codec IC.

In Data record, Aux record mode the digital audio data are send via I^2S bus to SFC3. Here, the broadband signal is separated into 32 subbands for left and right channels and a PASC frame is generated.
During PASC encoding the adaptive and scaling circuit (ADAS3) calculates the required accuracy (bit allocation) and scale factors of the PASC subband samples. The subband samples are transferred to ADAS3 via FDAI input port. The ADAS has to collect a complete frame of subband data before the allocation and scale factor information can be calculated. To have that information available in the same time frame as the audio samples are at the output, the subband filtered samples are delayed. (Dependant to the audio sample rate of 32, 44.1 or 48 kHz.) The delayed samples are passed to the codec part of SFC3 on the FDAO output port. This bus between SFC3 and ADAS3 in the recording mode is called the filtered data interface.

For every PASC frame the ADAS3 calculates a bit allocation and a scale factor table which is transferred to the SFC3. Once scaled the samples are re-quantized to reduce the number of bits to correspond with the allocation table, as calculated.
Synchronization, allocation and scale factor are added in SFC3 to provide a fully PASC data signal. These frames of data are now via 'SBI^{2}S-Bus' sent to the DRP.

The selection of decode or encode operation in the IC is controlled by the signals FRESET and FIDR. FRESET causes a general reset. The FDIR signal is sampled at the falling edge of the FRESET signal to determine the operation mode. When FDIR is HIGH SAA2013 is in decode mode. When FDIR is LOW the IC is in encode mode.

BLOCK DIAGRAM

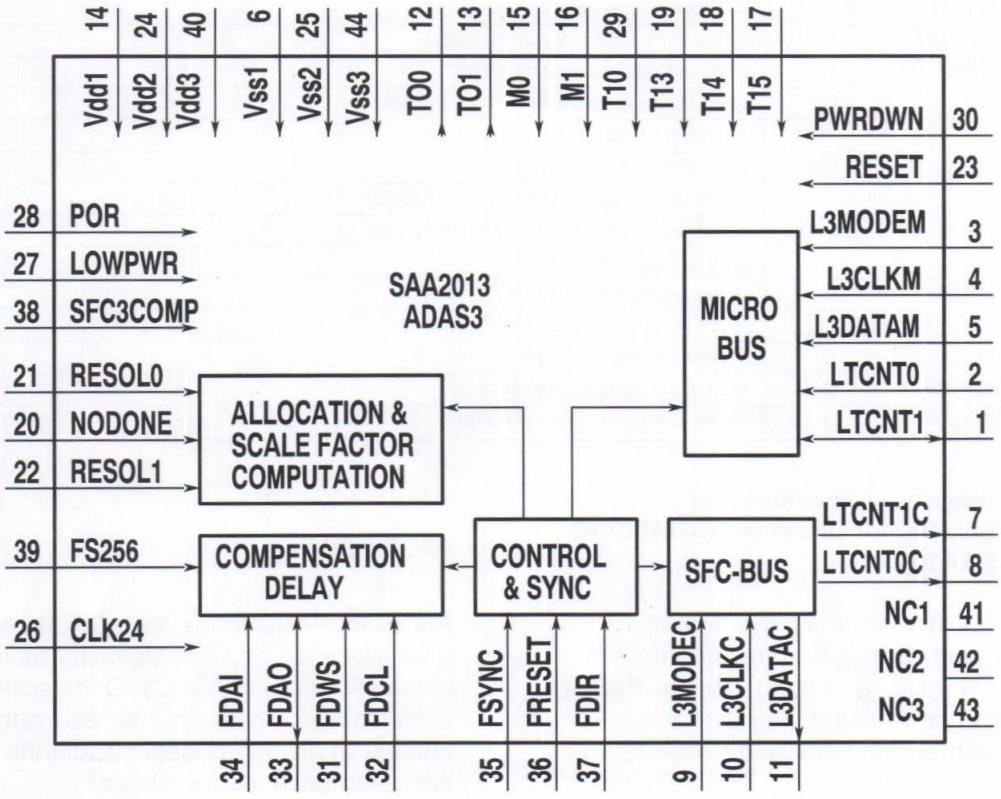

Fig. 26. SAA2013: Adaptive Allocation and Scalefactor Processor (ADAS3)

PIN CONFIGURATION SAA2013

PIN	NAME	I/O	FUNCTION
1	LTCNT1	I	ADAS interface mode control
2	LTCNT0	I	ADAS interface mode control
3	L3MODEM	I	microcontroller interface mode
4	L3CLKM	I	microcontroller interface clock
5	L3DATAM	I/O	microcontroller interface data
6	VSS	P	supply ground
7	LTCNT1C	O	SFC interface mode control
8	LTCNT0C	O	SFC interface mode control
9	L3MODEC	O	codec interface mode
10	L3CLKC	O	codec interface clock
11	L3DATAC	I/O	codec interface data
12	TO0	O	(test output)
13	TO1	O	(test output)
14	VDD	P	positive supply
15	M0	I	(test mode input) connect to VDD

16	M1	I	(test mode input) connect to VDD
17	TI5	I	(test input) connect to VSS
18	TI4	I	(test input) connect to VSS
19	TI3	I	(test input) connect to VSS
20	NODONE	I	No done state selection
21	RESOL0	I	resolution selection 0
22	RESOL1	I	resolution selection 1
23	RESET	I	active high reset input
24	VDD	P	positive supply
25	VSS	P	supply ground
26	CLK24	I	24.576 MHz clock input
27	LOWPOWER	I	Low power playback reset
28	POR	I	Power On Reset
29	TI0	I	(test input) connect to VSS
30	PWRDWN	I	power down input
31	FDWS	I	word select filtered-I^2S(F-I^2S) bus
32	FDCL	I	bit clock F-I^2S bus
33	FDAO	I/O	output data F-I^2S bus
34	FDAI	I/O	input data F-I^2S bus
35	FSYNC	I	subband synchronisation on F-I^2S bus
36	FRESET	I	reset signal from codec
37	FDIR	I	F-I^2S bus direction
38	SFC3COMP	I	SFC3(SAA2003) compatibility mode
39	FS256	I	system clock, 256x sample frequency
40	VDD	P	positive supply
41	NC		(not connected)
42	NC		(not connected)
43	NC		(not connected)
44	VSS	P	supply ground

3.2.5.4 Digital Audio Input/Output circuit(DAIO) IC TDA1315

This IC is a complete transceiver for bi-phase-mark encoded digital audio signal which are conform IEC958 interface standards (consumer mode).
In the receive mode, the device adjusts automatically to one of the 3 standardized sample frequencies (32, 44.1, 48 kHz), decodes the I^2S or IECIN0 input signal and separates audio and control data. A clock signal of either 256 or 384 times the sample frequency is generated to serve as a master clock signal in digital audio systems.
In the transmit mode, the device multiplexes the audio, control and user data and encodes it for subsequent transmission via a cable or optical link. (IECO)
In play back mode the audio broadband signal from SFC3 (SDA2 signal) is transferred via I^2S-interface to the DAIO (TDA1315). The DAIO, together with sub-code information of the Main µP, generates an IEC-958 signal, which is output via DIGITAL OUT.

In Data record, Aux record mode the audio data either reach the DAIO directly via DIGITAL IN (digital source), or are first digitized by the ADC (SAA7366) in case of an analog source. The DAIO converts the signal into I^2S bus format signal and the digital audio data are passed to SFC3.
In Data playback, Aux record mode there is no specific function for this IC.
In ACC playback mode the analog signal is fed to the Dolby IC CXA1331S, and after that the signal is digitized in the ADC. The DAIO generates (with the Main µP) an IEC958 signal, which is output via IEC OUT to DIGITAL OUT. The digital audio data are passed on to the DAC via the I^2S-interface of the DAIO, where they are D/A converted.

BLOCK DIAGRAM

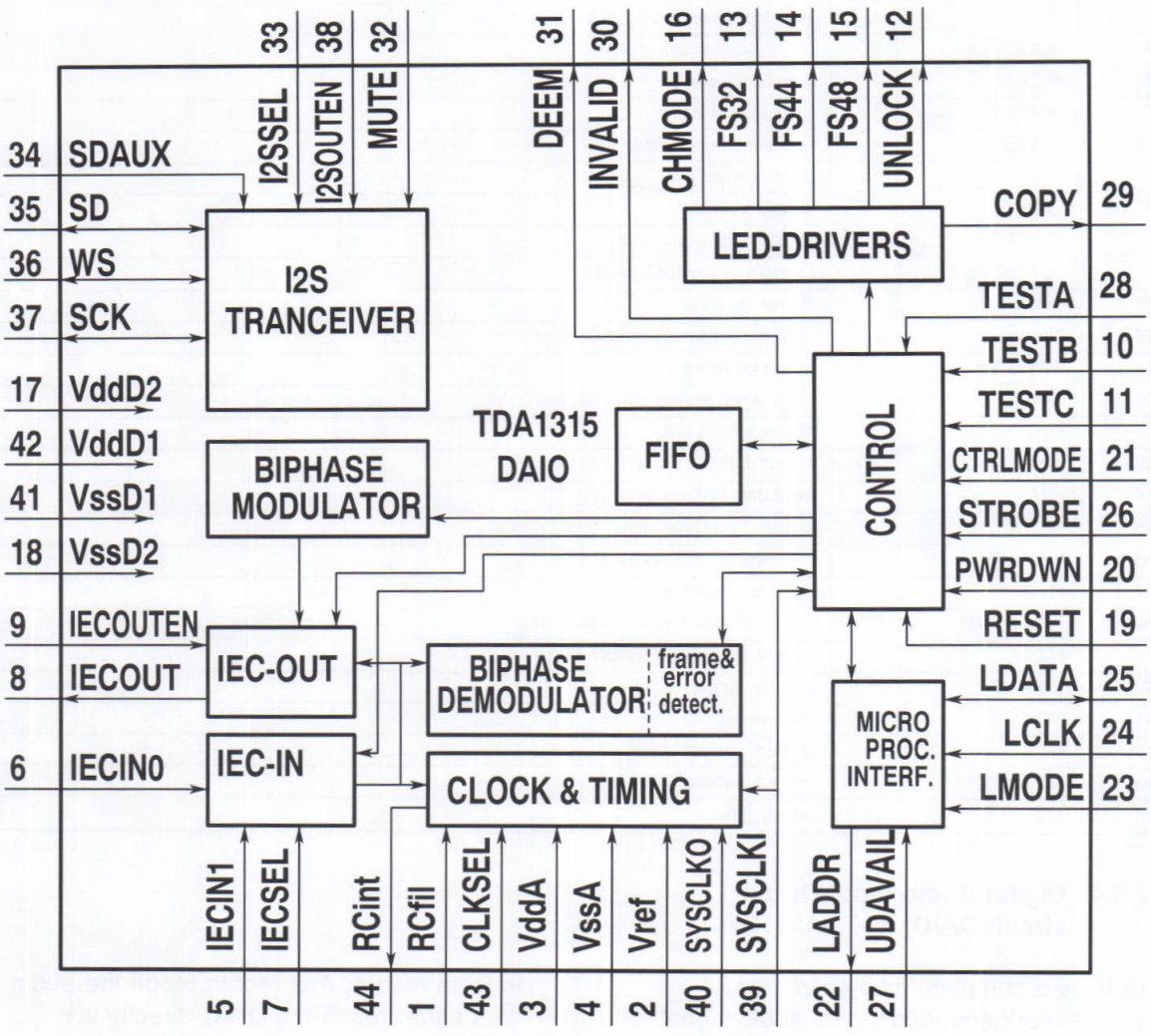

Fig. 27. TDA1315: Digital Audio Input/Output (DAIO)

PIN CONFIGURATION TDA1315

PIN	NAME	I/O	FUNCTION
1	RCfil	I	pin for PLL loop filter
2	Vref	P	pin for decoupling internal reference voltage
3	VddA	P	analog supply voltage
4	VssA	P	analog ground
5	IECIN1	I	high sensitivity IEC input
6	IECIN0	I	TTL level IEC input
7	IECSEL	I	select IEC input 0 or 1 (0=IECIN0, 1=IECIN1); (internal pull-up resistor)
8	IECO	O	digital audio output for optical and transformer link
9	IECOEN	I	digital audio output enable(0=enabled, 1=disabled/3-state)(internal pull-up)
10	TESTB	I	enable factory test input(0=normal application, 1=scan mode)
11	TESTC	I	enable factory test input(0=normal application, 1=observation outputs)
12	UNLOCK	O	PLL out-of-lock(0=not locked, 1=locked)

13	FS32	O	indicates sample frequency=32kHz
14	FS44	O	indicates sample frequency=44kHz
15	FS48	O	indicates sample frequency=48kHz
16	CHMODE	O	use of channel status(0=professional use, 1=consumer use)
17	VddD2	P	digital supply voltage 2
18	VssD2	P	digital ground 2
19	RESET	I	initialization after power-on
20	PWRDWN	I	enable power-down input in the standby mode
21	CTRLMODE	I	select μP/stand-alone mode(0=μP, 1=stand-alone)
22	LADDR	I	microprocessor interface address switch input
23	LMODE	I	microprocessor interface mode line input
24	LCLK	I	microprocessor interface clock line input
25	LDATA	I/O	microprocessor interface data line input/output
26	STROBE	I	strobe for control register(active high)
27	UDAVAIL	O	synchronisation for output user data(0=data available, 1=no data)
28	TESTA	I	enable factory (scan) test input
29	COPY	O	copyright status bit(0=copyright asserted, 1=no copyright asserted)
30	INVALID	I/O	validity of audio sample input/output
31	DEEM	O	pre-emphasis output bit
32	MUTE	I	audio mute input
33	I^2SSEL	I	select auxiliary input or normal input in transmit mode
34	SDAUX	I	auxiliary serial data input; I^2S-bus
35	SD	I/O	serial audio data input/output; I^2S-bus
36	WS	I/O	word select input/output, I^2S-bus
37	SCK	I/O	serial audio clock input/output; I^2S-bus
38	I^2SOUTEN	O	serial audio output enable
39	SYSCLKI	I	system clock input
40	SYSCLKO	O	system clock output
41	VssD1	P	digital ground 1
42	VddD1	P	digital supply voltage 1
43	CLKSEL	I	select system clock(0=384xfs, 1=256xfs)
44	RCint	O	pin for integrating capacitor

3.2.5.5 Digital/Analog Converter IC TDA1305

The TDA1305 is a filter-DAC, which combines bitstream and continuous calibration techniques. The converter functions as a bitstream converter for low signals while large signals are generated using the dynamic continuous calibration technique.
The IC is a Dital analog converter with upsampling filter and noise shaper. It is a combination of high oversampling up to $16F_s$, 2nd order noise shaping and continuous calibration conversion.

In the Data play back, Aux play back mode the audio broadband signal from SFC3 is transferred via I^2S-interface to the DAIO but also via a port extender to the DAC (TDA1305T).

The DAC converts the signal into analog audio signals LEFT and RIGHT which go to the appropriate analog outputs via buffer amplifiers.

In ACC playback mode the read audio signal is fed via Dolby IC to the ADC, where it is digitized. The digital audio data are passed on to the DAC via the I^2S-interface of the DAIO, D/A converted, and taken to the appropriate analog outputs via buffer amplifiers.

BLOCK DIAGRAM

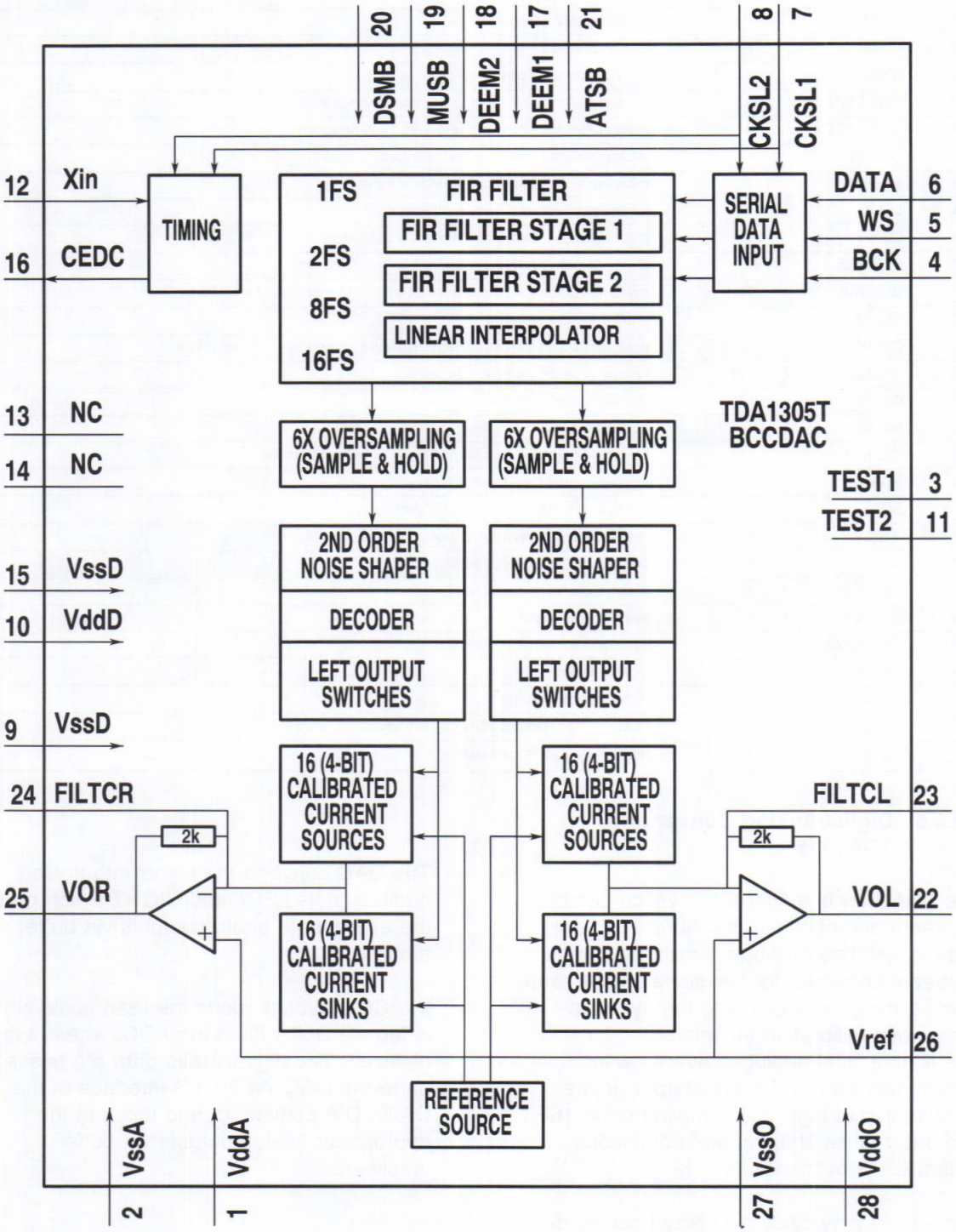

Fig. 28. TDA1305: Digital/Analog Converter (DAC)

PIN CONFIGURATION TDA1305

PIN	NAME	I/O	FUNCTION
1	VddA	P	analog supply voltage
2	VssA	P	analog ground
3	TEST1	I	test input; pin should be connected to ground.
4	BCK	I	bit clock input.
5	WS	I	word select input
6	DATA	I	data input
7	CKSL1	I	clock selection 1
8	CKSL2	I	clock selection 2
9	VssD	P	digital ground.
10	VddD	P	digital supply voltage.
11	TEST2	I	test input; pin should be connected to ground.
12	Xin	I	system clock input
13	NC		not connected
14	NC		not connected
15	VssD	P	digital ground
16	CEDC	O	system clock output.
17	DEEM1	I	de-emphasis on/off; DEEM 32kHz, 44kHz and 48kHz.
18	DEEM2	I	de-emphasis on/off; DEEM 32kHz, 44kHz and 48kHz.
19	MUSB	I	muting(active LOW)
20	DSMB	I	double speed mode(active LOW).
21	ATSB	I	12 dB attenuation(active LOW)
22	VOL	O	left channel output.
23	FILTCL	I	capacitor for left channel 1st order filter function, should be connected between this pin and VOL.
24	FILTCR	I	capacitor for right channel 1st order filter function, should be connected between this pin and VOR.
25	VOR	O	right channel output.
26	Vref	O	internal reference voltage for output channels(0.5xVdd)
27	VssO	P	operational amplifier ground.
28	VddO	P	operational amplifier supply voltage.

3.2.5.6 Analog/Digital Converter IC SAA7366

The SAA7366 is a bitstream conversion ADC for digital audio. The conversion is achieved by using a third order Sigma-Delta modulator, operating at 128 times the output sample frequency. The high oversampling ratio simplifies the design of the analog input anti-alias filter. The 1-bit code from the Sigma-Delta modulator is filtered and down-sampled (decimated) to 1 f_s in two stages of filtering. The output is according to I^2S bus configuration.

In Data record, Aux record mode the audio data either reach the DAIO directly via DIGITAL IN or OPTICAL IN (digital source), or are first digitized by the ADC (SAA7366) in case of an analog source. Via I^2S bus the digital audio data are passed to SFC3.

In ACC playback mode the analog read signal from the head is fed via the Dolby IC to the ADC, where it is digitized. The I^2S interface is connected to DAIO and DAC ICs.

BLOCK DIAGRAM

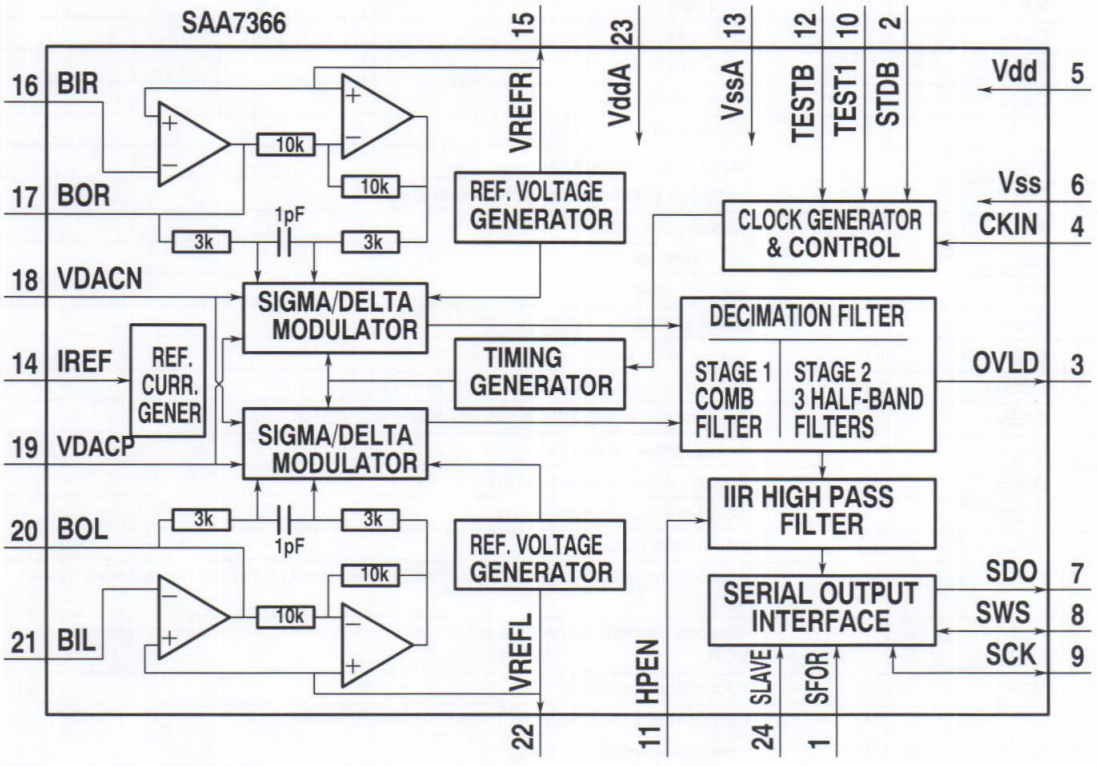

Fig. 29. SAA7366: Analog/Digital Converter (ADC)

PIN CONFIGURATION SAA7366

PIN	NAME	I/O	FUNCTION
1	SFOR	I	input for selecting serial interface output format.
2	STD	I	input for selecting STANDBY mode.
3	OVLD	O	overload indication output. This pin indicates whether the internal digital signal is within 1dB of maximum. In STANDBY mode this output is in high impedance.
4	CKIN	I	system clock input.
5	Vdd	P	supply for the digital section.
6	Vss	P	ground supply for the digital section.
7	SDO	O	serial interface data output.
8	SWS	I/O	serial interface word select signal. In MASTER mode this pin outputs the serial interface word select signal. In SLAVE mode this pin is the word select input to the serial interface. In STANDBY mode this pin is always an input(high impedance).
9	SCK	I/O	serial interface clock. In MASTER mode: serial interface bit clock output. In SLAVE mode: external bit clock input. In STANDBY mode: high impedance.
10	TEST1	I	test input 1.
11	HPEN	I	high pass filter enable input.(HIGH = enabled).
12	TEST2	I	test input 2.
13	VssA	P	ground supply for the analogue section.
14	IREF	I	current reference node.
15	VREFR	O	VddA/2 reference generator for the right channel analog section.
16	BIR	I	buffer op-amp inverting input for right channel.
17	BOR	O	buffer op-amp output for right channel.
18	VDACN	I	negative 1 bit DAC reference voltage input.(connected 0V)
19	VDACP	I	positive 1 bit DAC reference voltage input.(connected 5V)
20	BOL	O	buffer op-amp inverting input for left channel.
21	BIL	I	buffer op-amp inverting input for left channel.
22	VREFL	O	VddA/2 reference generator for the left channel analog section.
23	VddA	P	supply for the analog section.
24	SLAVE	I	input for selecting serial interface operating mode MASTER/SLAVE. HIGH = SLAVE, LOW = MASTER.

3.2.6 Digital Board Circuit diagram

Figure 21 shows the digital board circuit diagram, with the connections to other boards.

3.3 Tape drive control board

3.3.1 Block diagram

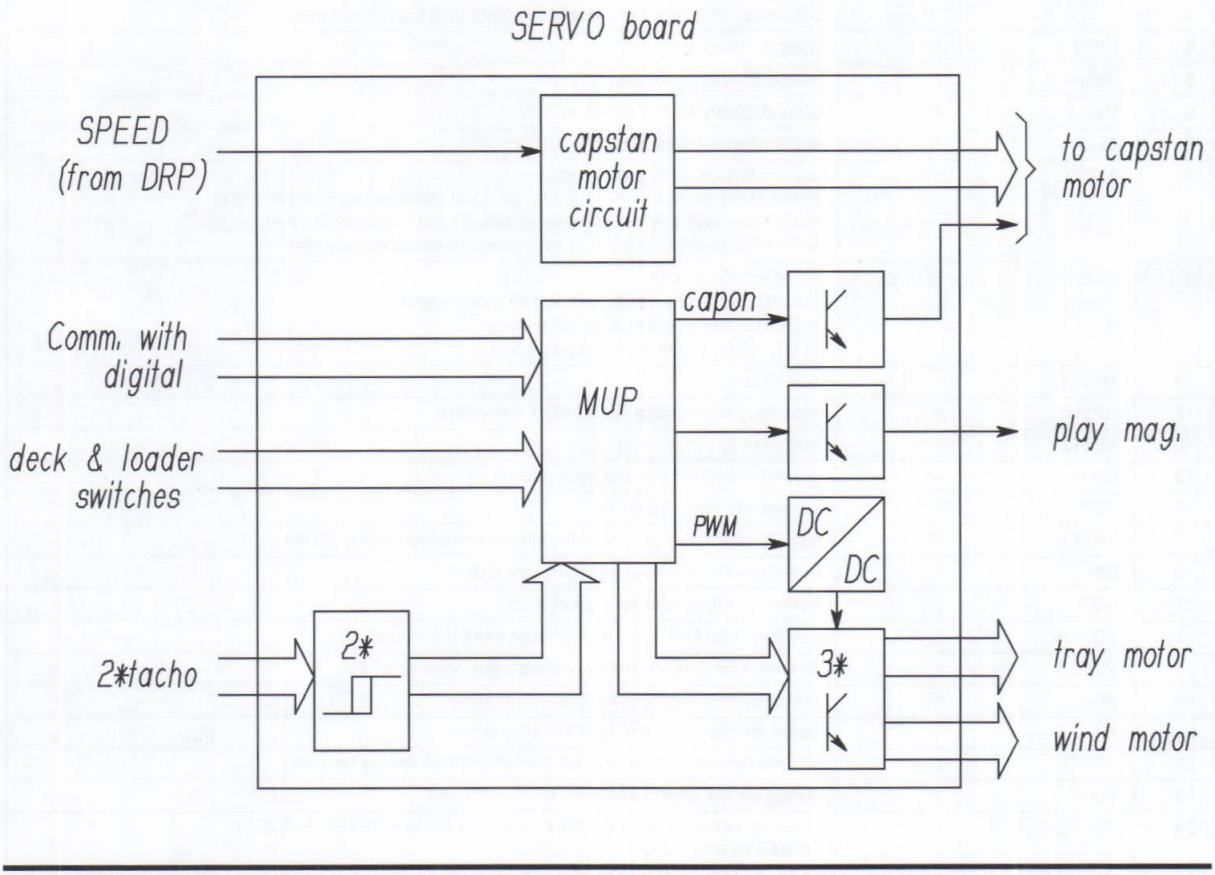

Fig. 30. Block diagram Tape Drive Control board DCC Digital Unit DDU

The Tape Drive board contains all electronics to control the CMRD deck of the DCC Digital Unit:

- Servo for activation of capstan motor
- Play-magnet activation
- Wind motor control (also for high speed winding, 50* play-speed)
- Tray control
- Signal conditioning for the reel sensor signals
- Micro processor

The capstan servo implements a phase lag regulator for the capstan motor servo loop in DCC playback mode.

The pulse width modulated signal 'speed', which carries phase- and velocity-information, is the input to the circuit, the output is the voltage between 'Cap_A' and 'Cap_B' on the capstan motor. (See block diagram figure 30 and circuit diagram figure 42.

In ACC playback and DCC recording, there are no speed information available, and the circuit sets the capstan motor to nominal speed (adjustable with potentiometer 3542 "A-side/sector" and 3543 "B-side/sector") #

Note: Item numbers within brackets refer to Tape drive control circuit diagram figure 42.)

To activate the capstan motor, there is a two transistor circuit (7540, 7541), which takes the 'N_CAPON' signal as input, and outputs a signal that makes the capstan motor run. (capstan+)

The play-magnet (Solenoid L101) activation is also done with a discrete transistor circuit (7563, 7564), connected to the microprocessor at pin 'N_SOL', and outputs a current to drive the play-magnet. This kind of circuit is not intended for driving a continued current through the magnet (only pulsed current).
'N_Solp' is active in search mode. The transistor circuit (7560, 7561, 7562 and diode 6560). The current through the solenoid is after the start pulse reduced to prevent heating of the solenoid. The current can be decreased because there is only a small force needed to maintain that search position.

The reel motor control is achieved by the IC BA6246 (7580), which is a power driver which is connected to the Tape Drive Control μP (7500) with three select wires (Driver S0, Driver S1, Driver S2). The driver IC controls the reel motor (Wind Motor M101) in both directions and the voltage across the motor is equal to the voltage at pin 'Vr'. As the voltage supplied to the reel motor is allowed to be 16 V, and there is only one 10 V supply to this board, a DC/DC-converter 'MC34063AP1' is used to generate a supply voltage up till 17 V. The reel motor voltage is controlled by the applied pulsed voltage of the microprocessor at pin 'WIND_SPEED'. This pulsed voltage is then integrated, amplified and presented to the 'Vr' pin on the driver IC by a circuit that also generates a signal that always keeps the output voltage of the DC/DC-converter higher than that on the 'Vr' pin.

Opening and closing of the tray loader (by tray motor M81) is also achieved by the same motor driver IC (7580) as it is a complete two motor driver.

There are also two comparators (LM324AD) with hysteresis which convert the slow changing impulses from the reels (TReel, SReel) to a well defined signal which can be accepted by the micro processor.

3.3.2 Control Timing charts

3.3.2.1 Functions of DCC tape deck 'CMRD'

1. FORWARD PLAY / (REC)
2. REVERSE PLAY / (REC)
3. FF-SEARCH
4. REW-SEARCH
5. STOP (PAUSE)
6. FF
7. REW

3.3.2.2 Operation

As already described in chapter 2.2 Command gearwheel, there are three main modes of STOP, PLAY, SEARCH in the tape deck operation. Each position is cyclically obtained by rotating of the 'intermittent' command gearwheel. The flywheel delivers the power to the mechanism and the start of each activity is triggered by a solenoid. In figure 31 the cycle is shown. From STOP the deck goes e.g. into the Forward PLAY mode and after that in the 'A head SEARCH' mode. The SEARCH mode is kept by supplying a continuous voltage to the solenoid.

The 2 head-position facilities like FORWARD and REVERSE are obtained during the move from STOP to PLAY and controlled by the solenoid L101.
Selections of these head modes are determined by interrupting the supplied voltage to the solenoid or not.
The Head direction in the SEARCH mode is the same as that of the head in the PLAY mode.
FF and REW operations are performed by the rotating reel motor in forward or reverse direction.

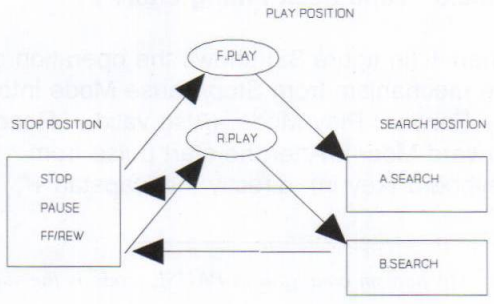

Fig. 31. Tape deck operations

3.3.2.3. Operation Control Matrix

			NEXT MODE								
			STOP	F.PLAY	R.PLAY	FF	REW	A HEAD SEARCH		B HEAD SEARCH	
								FF	REW	FF	REW
PRESENT MODE	STOP[4]		\[5]	1	2	3	4	\	\	\	\
	F.PLAY		5	\	6	\	\	7	8	\	\
	R.PLAY		5	9	\	\	\	\	\	10	11
	FF		12	\	\	\	\	\	\	\	\
	REW		12	\	\	\	\	\	\	\	\
	*[6] A HEAD SEARCH	FF	13	14	15	\	\	\	16	\	\
		REW	13	14	15	\	\	17	\	\	\
	* B HEAD SEARCH	FF	13	14	15	\	\	\	\	\	16
		REW	13	14	15	\	\	\	\	17	\

3.3.2.4 Initialization

First of all the command gearwheel must be shifted to the STOP position as it is being rotated at free position.
After power on of the set, the mechanism is initialized according to the FLOWCHART as shown in figure 32.

3.3.2.5 Timing charts

The mechanism is controlled according to TIMING CHART as shown in next chart drawings. The unity of time is msec.
To keep the mechanism's actions exactly, the tape speed must be as specified.
To explain the charts a few examples are described.

3.3.2.6 Tape deck timing chart 1

Chart 1 (in figure 33) shows the operation of the mechanism from Stop/Pause Mode into the Forward Play Mode. (Also valid in Record forward Mode). After the start pulse from keyboard (key in), directly the 'capstan +', 'wind speed' and 'Inhibit MSync' -signal lines are activated. This means capstan motor starts, Winding motor starts and the Messages synchronization has been blocked for new inputs. After a fixed delay, (depending on the mass of the flywheels, 100 msec for moulded flywheels, 150 msec for dycasting or sintered flywheels) the capstan has obtained its nominal speed and the solenoid is activated, resulting in the moving of the command gear wheel to the forward play position. Also the reel motor DC/DC circuit has generated the reel supply voltage and M101 is driven via 'Wind+' signal and obtains its nominal speed. Than capstan motor M102 is controlled by 'CAP A' signal and obtains its playback speed and transports the tape along the head. To close the procedure 'Inhibit M Sync' signal becomes LOW and finally 'N Mute'is switched off.

3.3.2.7 Tape deck timing chart 7

Chart 7 (in figure 36) shows the operation of the mechanism from Forward Play Mode into the Forward Search Mode. (A side/sector).

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[4] *Mechanism condition in PAUSE mode is the same as STOP mode.*

[5] *The figures in the table indicate the correspondent CHART NUMBER, and those matrixes with no CHART NUMBER are not able to change to the other mentioned mechanism mode directly.*

[6] ** 'A HEAD SEARCH' applies to the HEAD direction in FORWARD PLAY position, and 'B HEAD SEARCH' applies to REVERSE PLAY position.*

After the start pulse from keyboard ('key in' signal) the solenoid is directly started ('SOL' signal). The capstan motor ('capstan +' signal) is delayed switched off. Via the command gear wheel the head support assembly in now brought in the search position. After a small pause (see 'wind+' signal) the wind motor transports the tape along the head controlled by the 'Wind speed' signal. The audio output is muted by 'N Mute'. After the first 'SOL' impulse to the solenoid the 'SOL P' circuit becomes active and maintains the search position as long as desired. Moving from play to fast forward search the 'M Sync' signal line is inhibited.

Signal lines explanation:

Key in	:	Activation of the procedure by customer via key contact.
SOL	:	Control signal used for solenoid as trigger or status hold
M102 (Capstan +)	:	Capstan drive Motor M102
M102 (CAP A)	:	Capstan Motor rotation speed switching ('H': Stands for double speed). When changing mode, always set to 'L', and also if the double speed mode will not be used, set to 'L'.
M101 (Wind +)	:	Reel motor; M101 (Wind +) indicates forward direction.
M101 (Wind -)	:	The same as M101 (Wind +) but now for rewind directions.
Windspeed	:	Wind speed supply power control signal of Reel motor: 'H' applies a voltage corresponding to PLAY torque to the reel motor, and 'L' corresponding to FF / REW torque.
Inhibit (M Sync)	:	Mode shift operation to next mode is inhibited for this period when switching to next mode.
N Mute	:	Control signal to activate the mute circuit. N indicates that 'L' is the active mute signal.
SOL P	:	Controls an applying voltage to hold SEARCH mode and to prevent overheating of the solenoid.

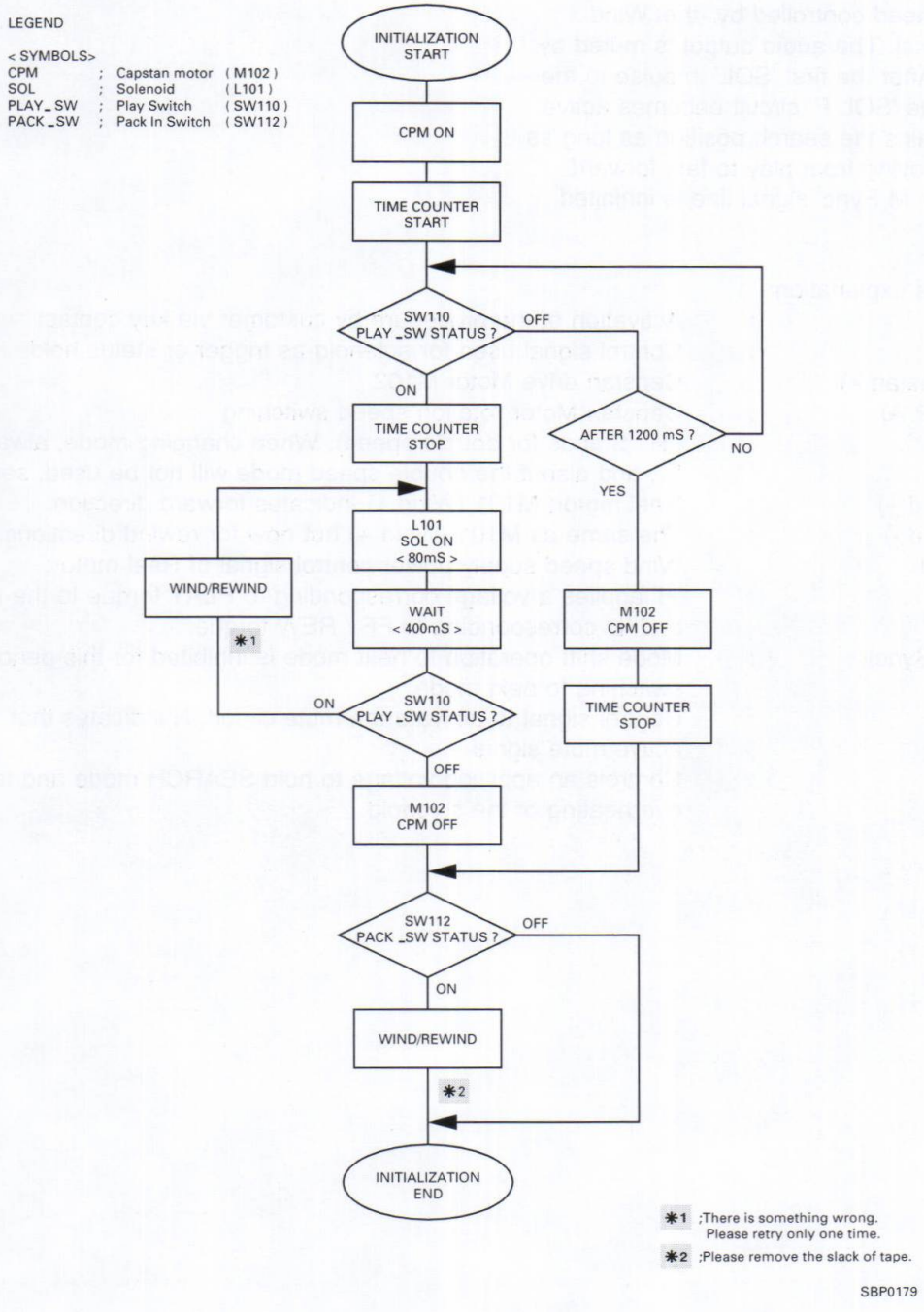
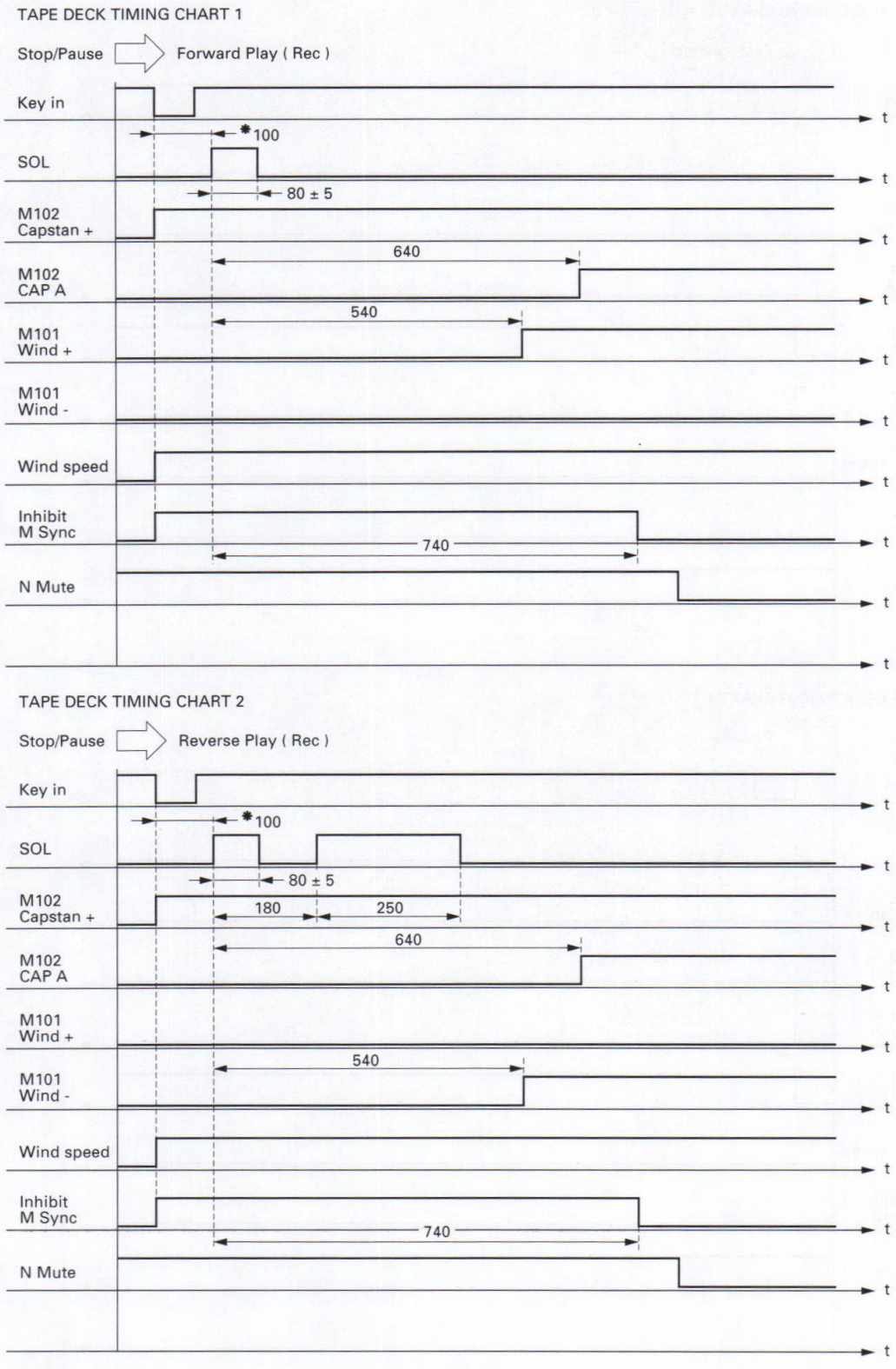


Fig. 32. Flow chart tape deck timing



* This timing is the data when mold flywheels are used.
Please change to more than 150 mS at Zn-diecasting or sinterd flywheels.

SBP0180

Fig. 33. Tape deck timing charts

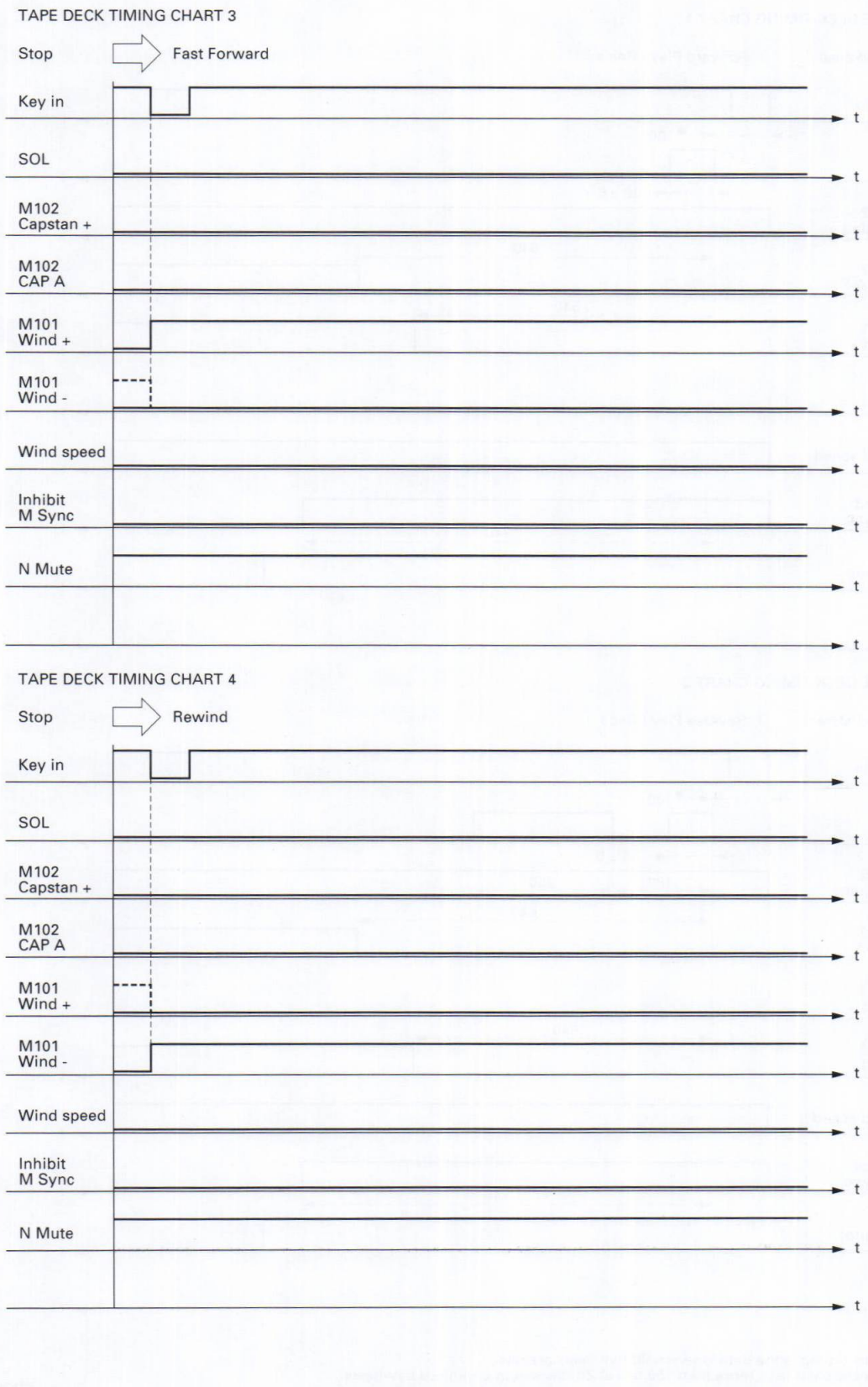
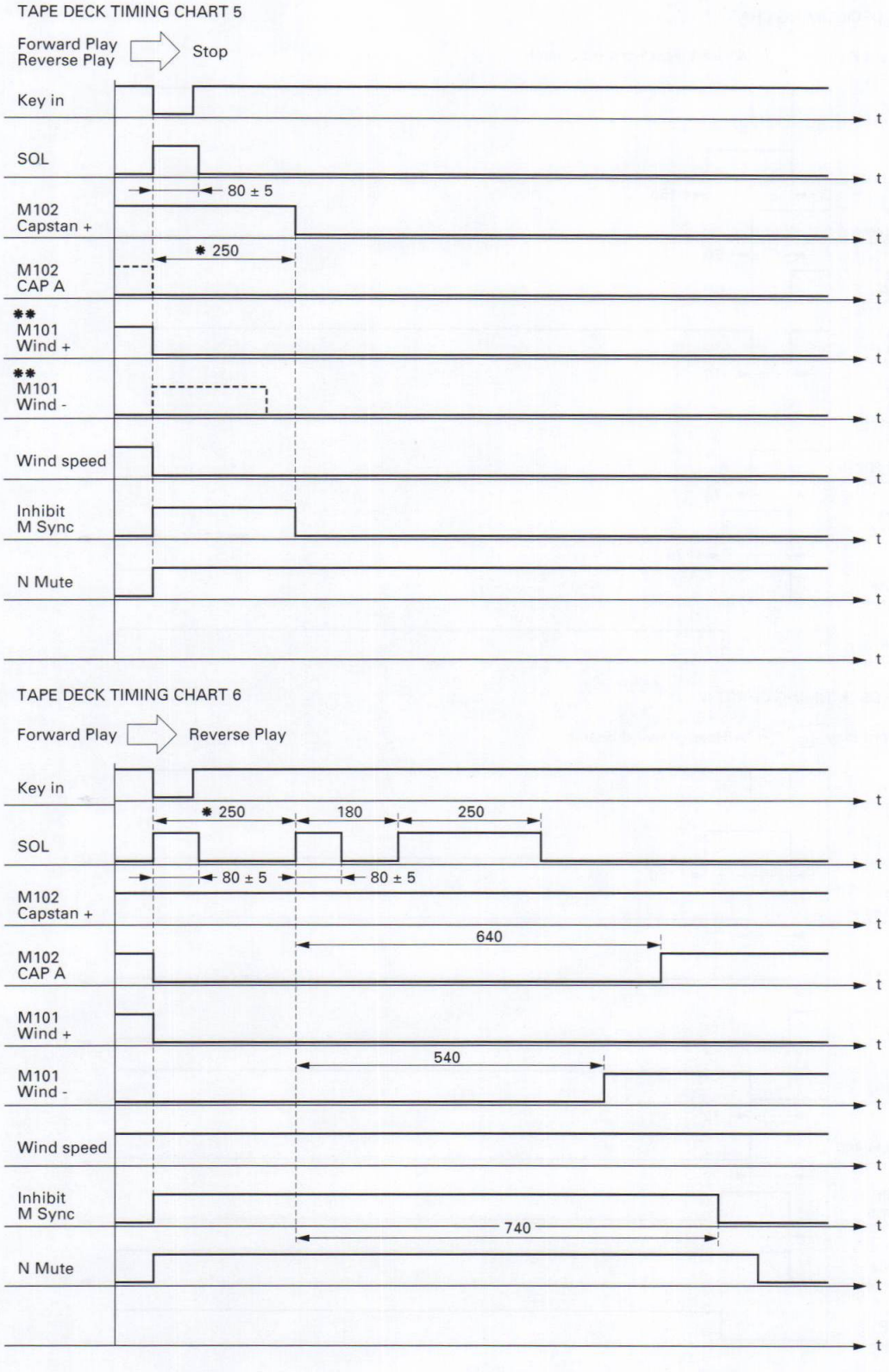


Fig. 34. Timing charts



* Please change 250mS to 400mS at double speed PLAY mode.
** Interchange M101 Wind + and M101 Wind - timing at REVERSE PLAY mode.

SBP0182

Fig. 35. Timing charts

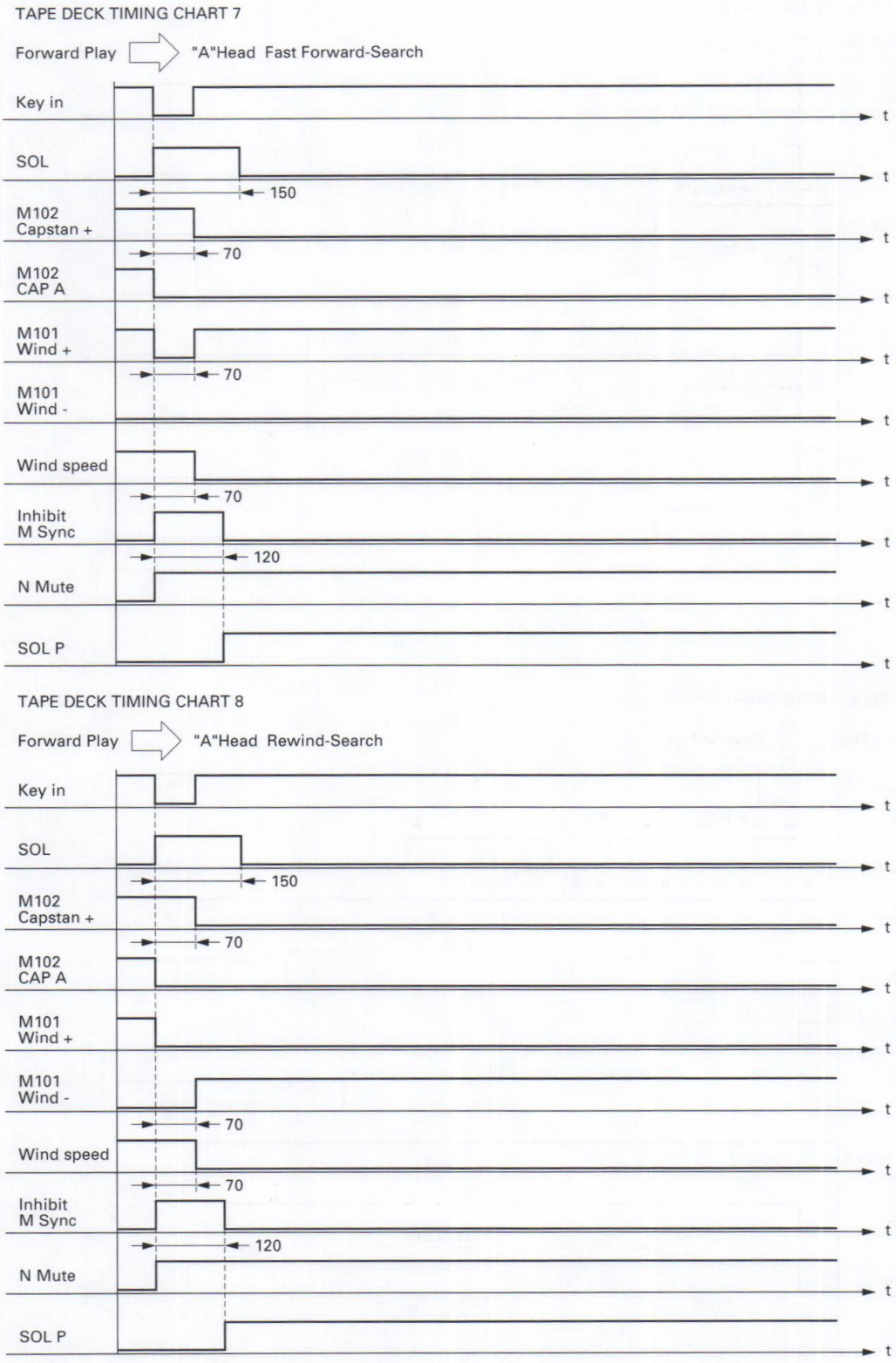
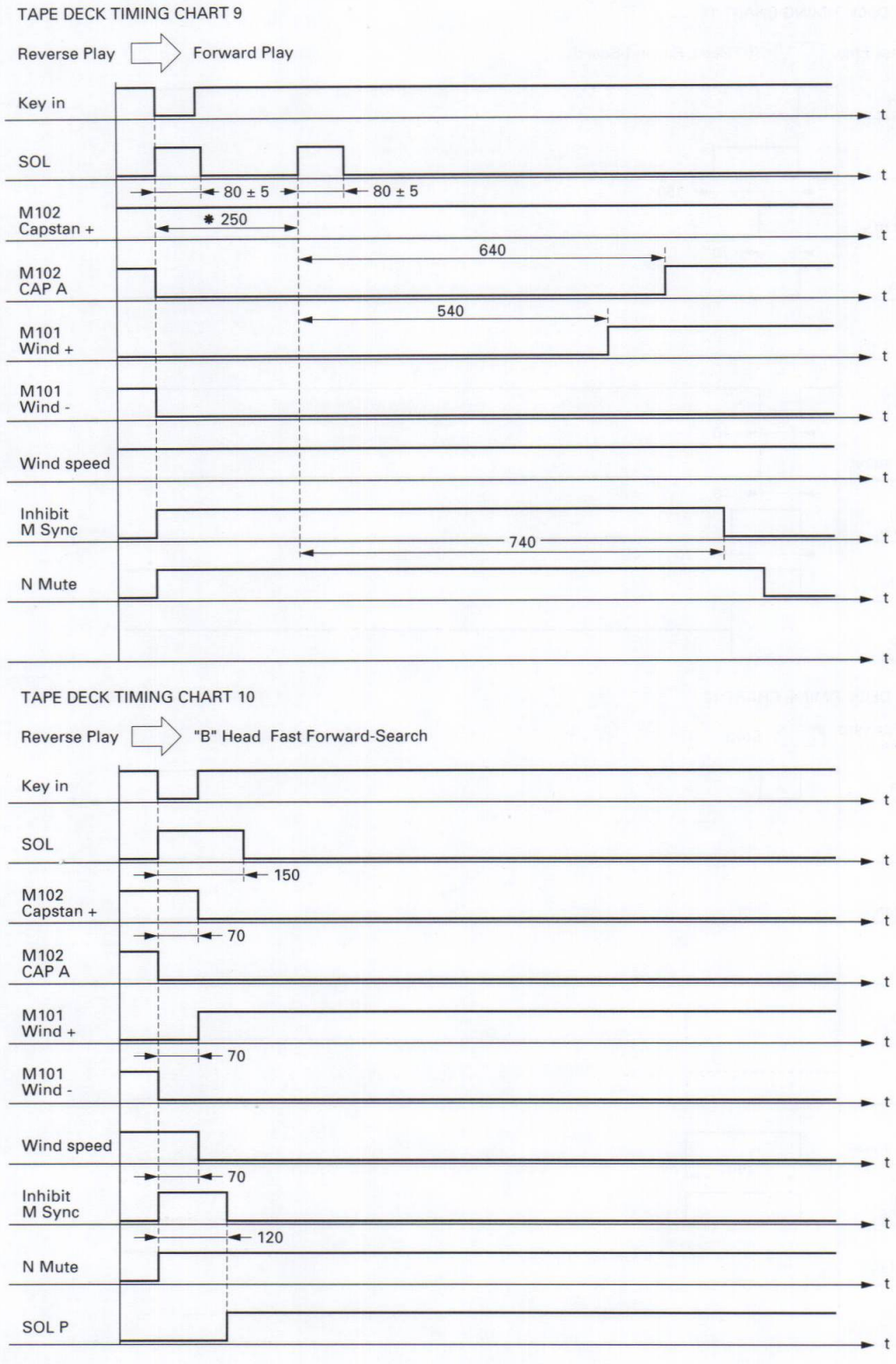


Fig. 36. Timing charts



* Please change 250mS to 400mS at double speed PLAY mode.

SBP0184

Fig. 37. Timing charts

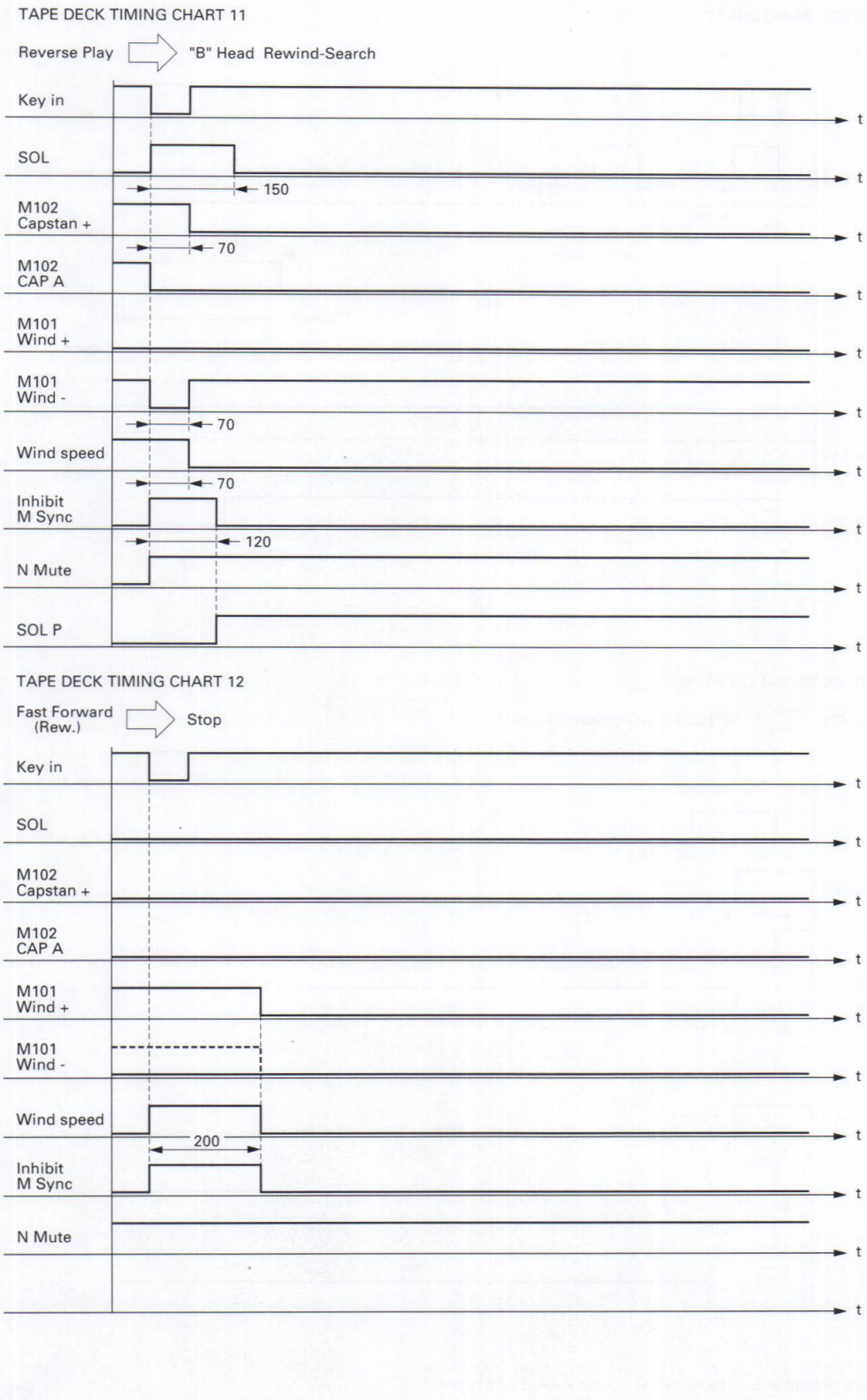


Fig. 38. Timing charts.

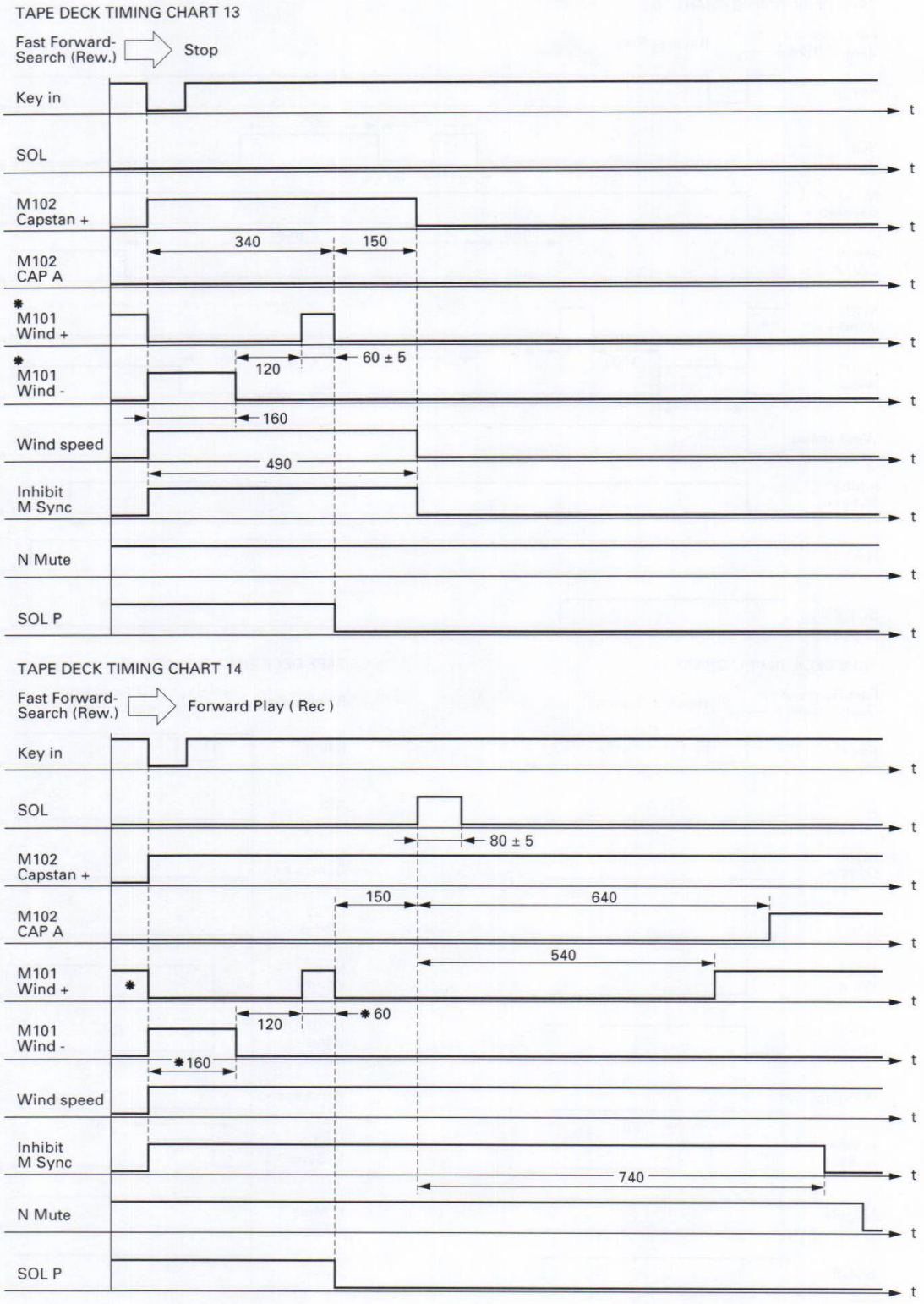


Fig. 39. Timing charts.

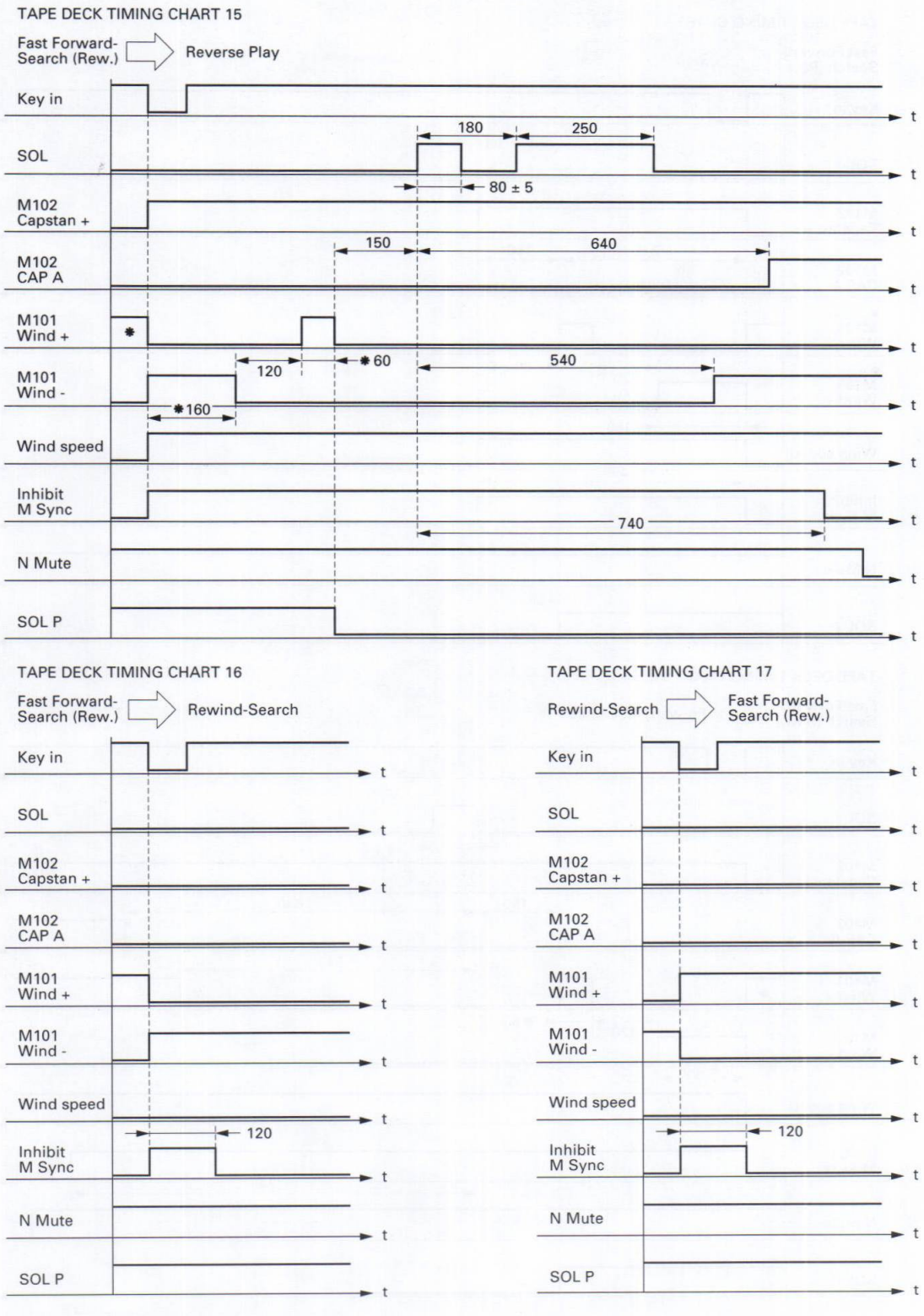


Fig. 40. Timing charts.

3.3.3 Pin configurations of Tape Drive Control Board Connectors

Item:	Pins:	Function:
1501	5	Loader interface
1502	14	Reel detector and DCC switch interface
1503	4	Reel motor and solenoid interface
1504	4	Capstan interface
1505	11	Tape Drive Controller interface

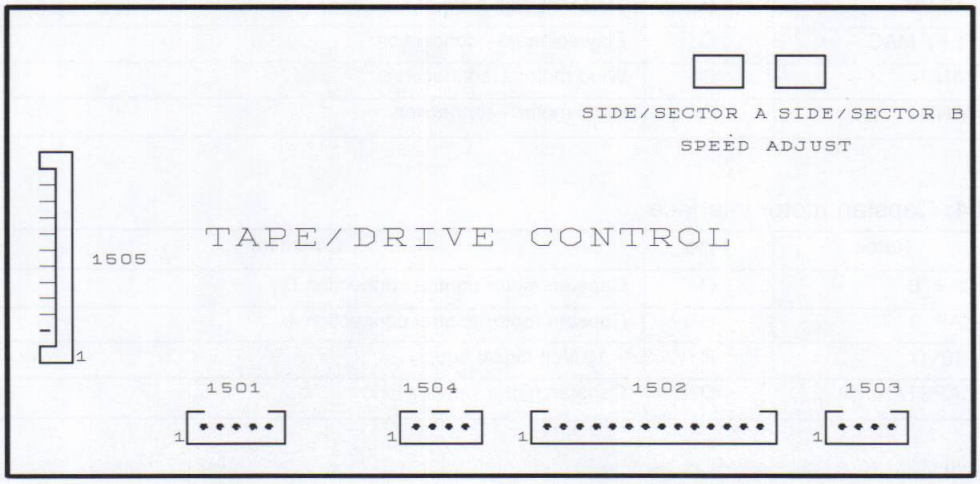


Fig. 41 Tape Drive Control Board connectors

Connector 1501: Loader interface

Pin No.	Name	Type[7]	Comment
1	CLOSE_TRAY/FLAP_OPEN	O	Tray motor connection (+10V = close Tray; 0V = open Tray)
2	OPEN_TRAY	O	Tray motor connection (+10V = open Tray; 0V = close Tray)
3	N_TRAY_IN	I	Tray switch input (L = Tray Loader in)
4	GNDS	P	Analog motors ground
5	N_FLAP_OPEN	I	Indicates if flap loader is open.(if CMRD is equipped with flap loader).

Connector 1502: Switches & sensors interface

Pin No.	Name	Type	Comment
14	N_PLAY_POS	I	Indication if head is in PLAY position
13	GNDD	P	Digital ground
12	+5VD	P	+ 5 Volt digital supply
11	QUICK REVERSE	I	Quick reverse sensor input signal
10	N_QREV_PRES	I	Indication if mechanism is equipped with QR sensor
9	N HOLE5	I	DCC tape length indication switch input (active Low)

[7]*Note: P= Power; I= Input, aI= Analog Input; O= Output; aO= Analog Output; I/O= Input/Output*

8	N HOLE4	I	DCC tape length indication switch input (active Low)
7	N HOLE3	I	DCC tape length indication switch input (active Low)
6	N DCC REC PROT	I	DCC record protect switch input (active Low)
5	DCC CAS PRES	I	DCC cassette present switch input (active High; H = DCC, L = ACC)
4	CRO2	I	CRO2/FE cassette detection switch input (L = FE; H = CRO2)
3	N CASS PRES	I	Cassette present switch input (L = cassette present)
2	SREEL	I	Tacho Supply reel
1	TREEL	I	Tacho Take-up reel

Connector 1503: Reel motor & solenoid

Pin No.	Name	Type	Comment
4	+10 VD	P	+ 10 Volt digital supply
3	PLAY MAG -	O	Play solenoid - connection
2	WIND+	O	Wind motor + connection
1	WIND-	O	Wind motor - connection

Connector 1504: Capstan motor interface

Pin No.	Name	Type	Comment
4	CAP_B	O	Capstan motor control connection B
3	CAP_A	O	Capstan motor control connection A
2	+10VD	P	+ 10 Volt digital supply
1	CAPSTAN-	O	Capstan motor - connection

Connector 1505: Tape Drive controller interface

Pin No.	Name	Type	Comment
11	GNDD	P	Digital VSS
10	NDCC-REC-PROT	I	DCC record protection switch input
9	RXD	I	Serial data input from tape drive unit (L = Record protect)
8	+5VD	P	+5 Volt digital supply input
7	TXD	O	Serial data output to tape drive unit
6	SPEED	O	Analog control signal for capstan control
5	RESET_UP	O	Reset tape drive module µP
4	+10VD	P	10 volt digital supply input
3	GNDS	P	Analog motors ground
2	N_FAILP	O	Power fail (L = power failure)
1	MSYNC	I/O	Message synchronisation with Digital µP

3.3.4 Tape Drive Control Circuit diagram

In figure 42 the Tape Drive Control Board Circuit diagram is shown, with the interconnections within the board, the connections to other boards and the connections to the tape deck mechanism.

67 CIRCUIT DESCRIPTION

TAPE DRIVE CONTROL CIRCUIT DIAGRAM

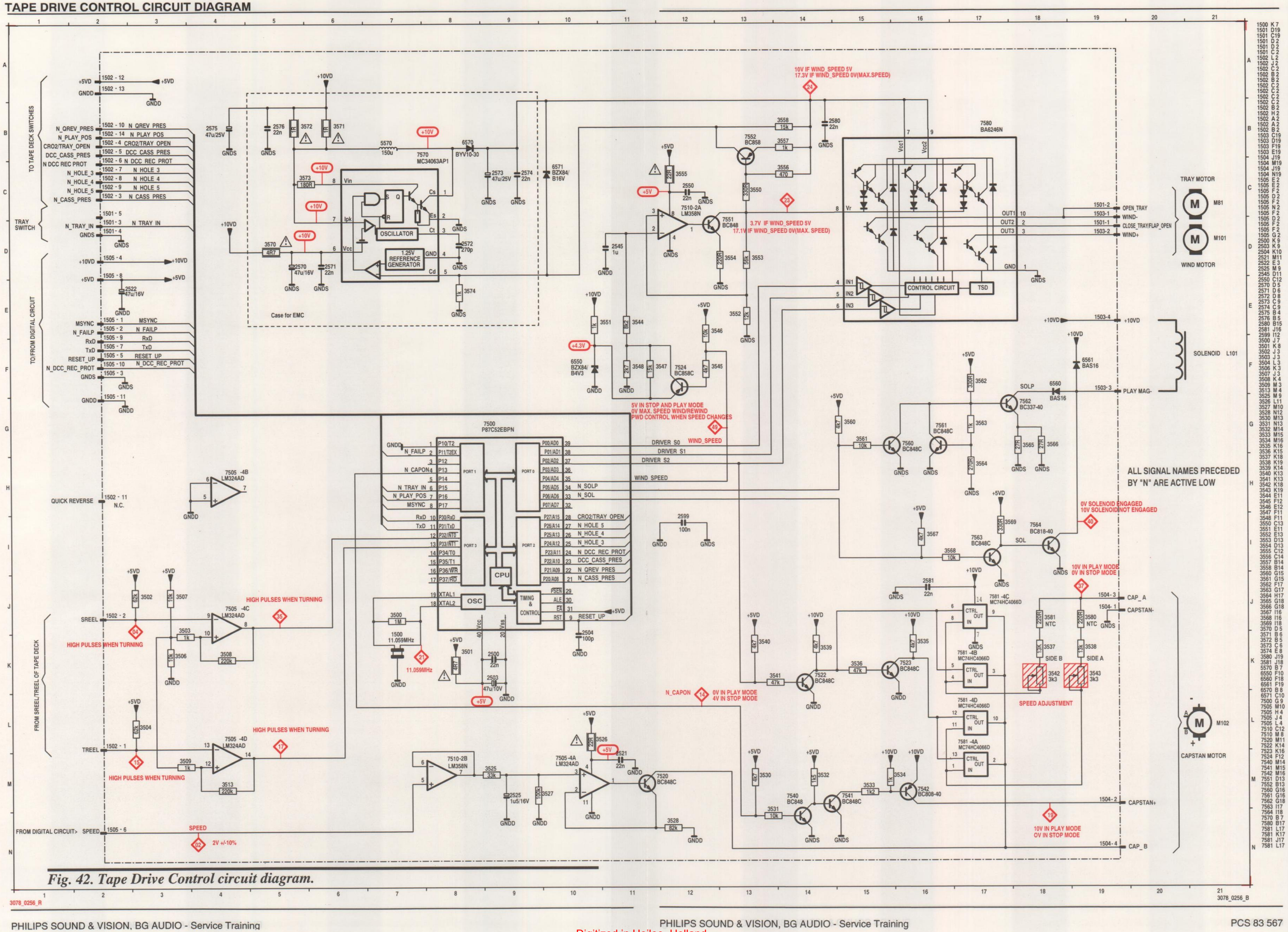


Fig. 42. Tape Drive Control circuit diagram.

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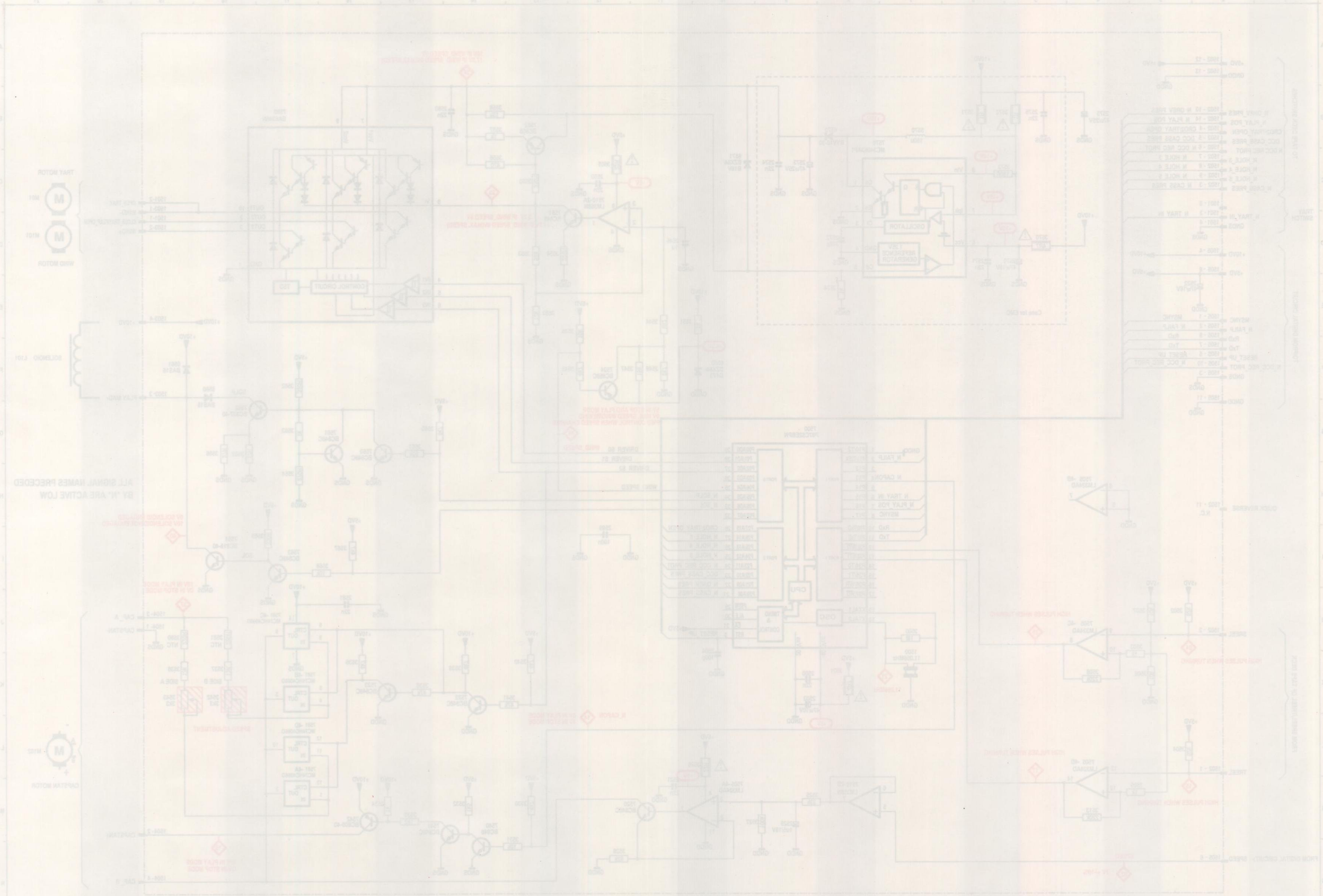
CIRCUIT DESCRIPTION 68



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4. INTERFACE

The electrical interface part of the DCC951 recorder consists of:
- o Power Supply
- o In /Out Signals
- o Control & Display

Via a few details of the circuit diagrams some interface functions are highlighted. Please notice that this interface part can deviate per set.

4.1. Power Supply

In the recorder the following supply voltages are generated in the secondary circuit:
- + and - 10 V Rectification
- + 5 V Rectification
- FTD Voltages: VFTD, VAC1 and VAC2
- Kill and powerdown circuit

The KILL and powerdown circuit has been shown in detail in figure 43.

Switch on the power supply and measure immediately after power on the voltage on point **F**.

point **F** = + 3V. (measuring point 1 in power supply circuit diagram figure 44)

Check that point **F** drops to -8V after a short while. Then Kill is no longer active.
Check also point **E** and **G** in this status.
point **E** = + 4.5V
point **G** = + 5V. (measuring point 2 in power supply circuit diagram figure 44)

Switch off the power supply (Power off) and check that point **G** switches over to 0V.
point **G** = ± 0V. (measuring point 2 in power supply circuit diagram figure 44)

In figure 44 the Power Supply circuit diagram is shown.

4.2. In / Out board.

In the In /Out board the following circuits are located:
- Amplifying of the Analog In signal (Record Mode)
- Amplifying of the Analog out signal (Playback Mode)
- Digital In (Record Mode)
- Optical In (Record Mode)
- Digital Out (Playback Mode)

In figure 45 the In/Out circuit diagram is shown.

The amplifier stage of analog output circuit in playback mode has been shown in detail in figure 46.
When the DCC General purpose test cassette (4822 397 30256) is inserted and track 10 is chosen in repeat mode, a 1 kHz (0 dB) signal is (hardly) continuously fed to the Analog output stage.

Points **A** and **B** = 1 kHz 4Vpp (peak to peak) with an DC-offset of +2V. (See also measuring points 91 and 92 on In/Out circuit diagram, figure 45)
Check the function of DAC IC in case this signal deviates.
On the following measuring points the next signals will be measured:

Point **F**, **P** = 1kHz 6Vpp with DC-offset of -3V. (Points **F** and **P** correspond with Measuring points 93 and 94 on In/Out circuit diagram, figure 45)

Points **G** and **Q** = 1 KHz 5Vpp.
(Points **G** and **Q** correspond with Measuring points 95 and 96 on In/Out circuit diagram, figure 45)

4.3 Control & Display Board

In figure 47 the Control & Display circuit diagram is shown.

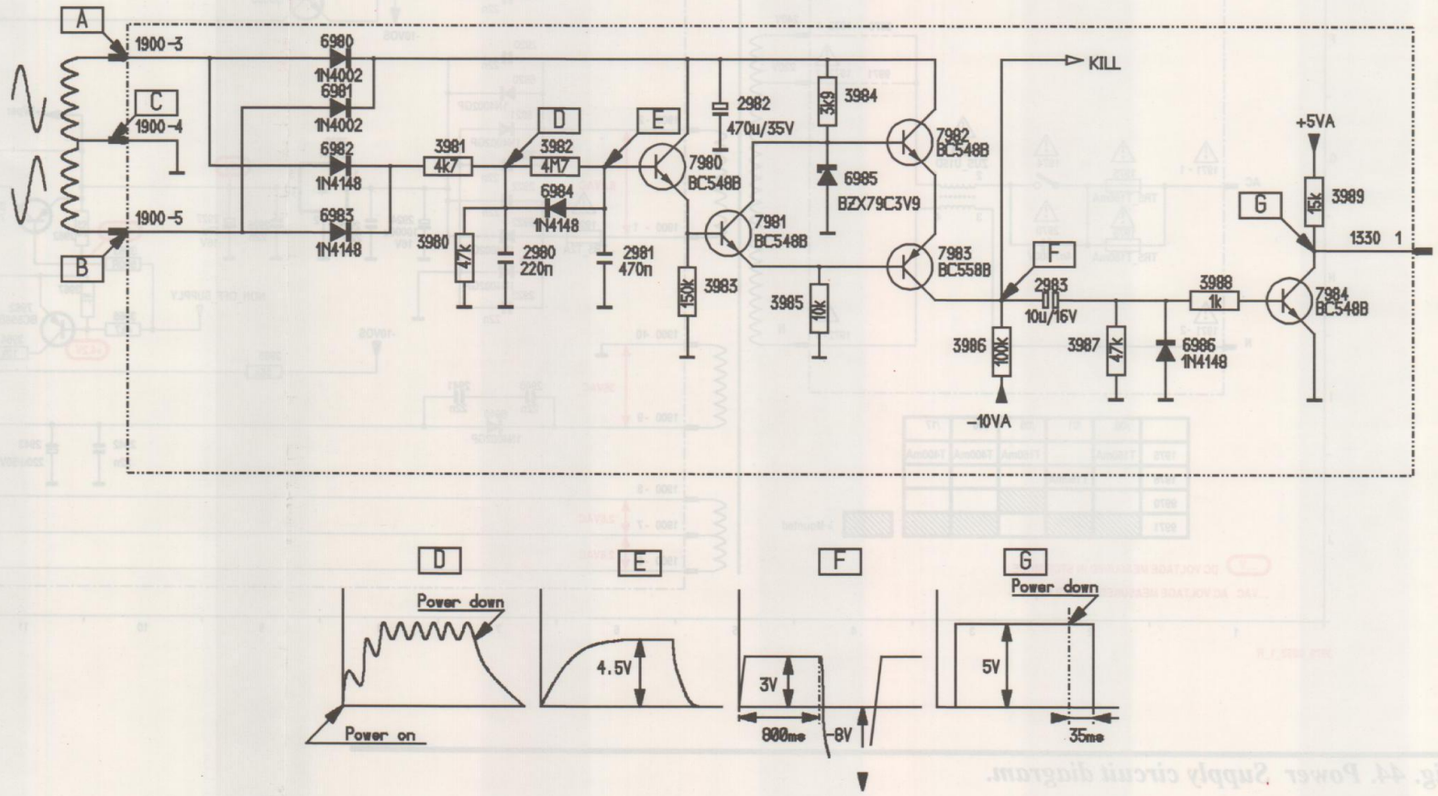

Fig. 43. Measuring lay-out for kill and powerdown.

CIRCUIT DESCRIPTION 70

POWER SUPPLY CIRCUIT DIAGRAM

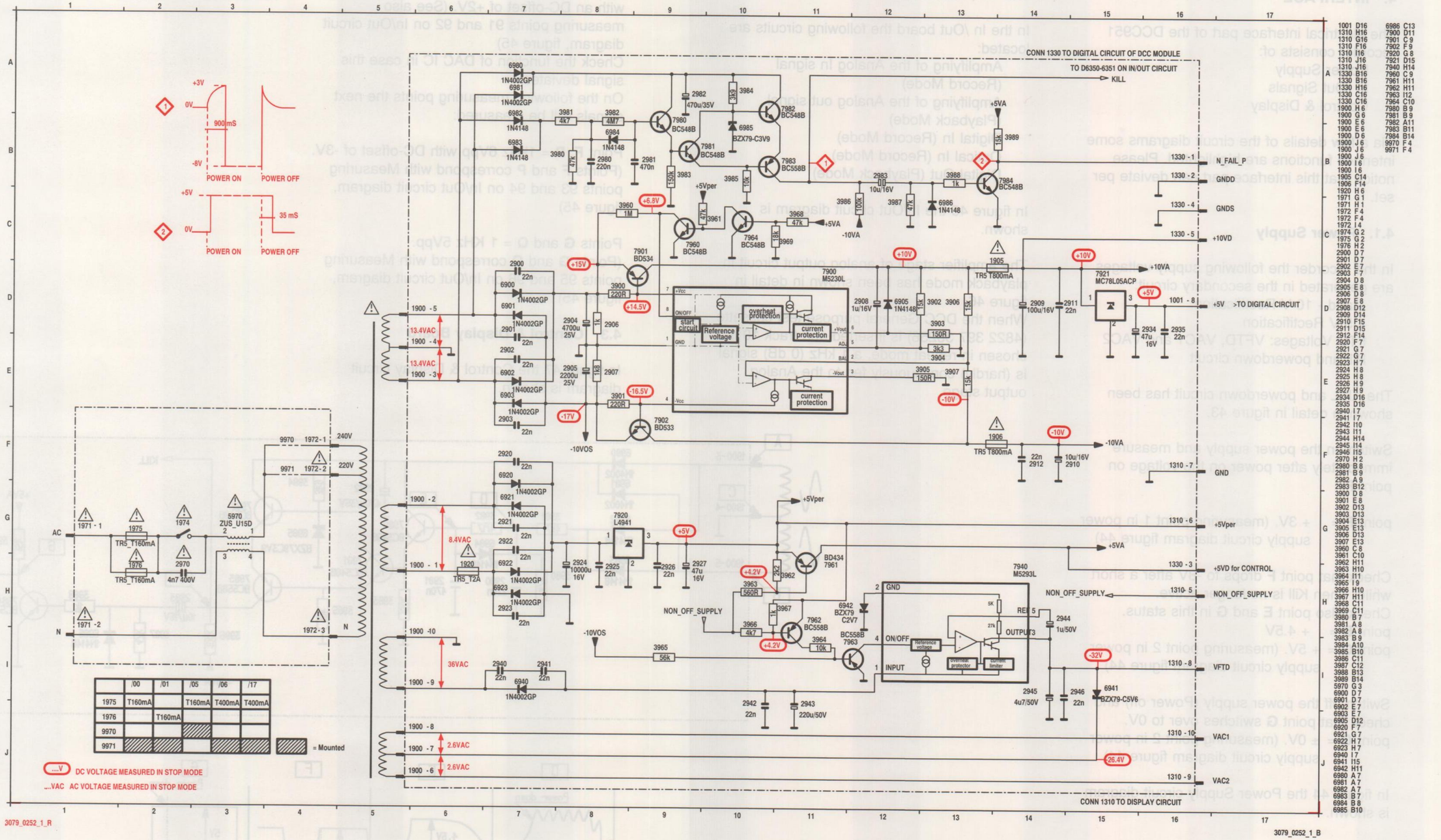

Fig. 44. Power Supply circuit diagram.

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71 CIRCUIT DESCRIPTION

ANALOG IN REC

ANALOG OUT PLAY

DIGITAL OUT PLAY

DIGITAL IN REC

SYSTEM CONTROL ESI BUS

TO LEVEL CIRCUIT

FROM LEVEL CIRCUIT

LEFT IN

GND

RIGHT IN

+10V

-10V

RIGHT OUT

LEFT OUT

TO ADC ON DIGITAL CIRCUIT

FROM MICRO CIRCUIT>

MICRO_IN

TO DISPLAY CIRCUIT

NHIGH_LOW_REC_LEVEL

NMICRO_ANA_REC

FROM DAC ON DIGITAL CIRCUIT

DACL

NMUTE

NMUTER

DACR

FROM DAIO ON DIGITAL CIRCUIT

DIG OUT

+5V

DIG/OPT

+5VDS

LHP >TO HEADPHONE CIRCUIT

RHP

-8V PLAY MODE
+5V STOP MODE

KILL

TO MICRO & HEADPHONE CIRCUIT

NMICRO_DET >TO DISPLAY CIRCUIT

DIGITAL IN

OPTICAL IN

TO DAIO ON DIGITAL CIRCUIT

ESI IN

DIGITAL DETECTION

ESI OUT

TO DISPLAY CIRCUIT

ONLY DCC951

2V 4Vpp 2ms/DIV GENERAL PURPOSE TEST TRACK 10 1KHz 0dB

-3V 6Vpp 2ms/DIV GENERAL PURPOSE TEST TRACK 10 1KHz 0dB

0V 5Vpp 2ms/DIV GENERAL PURPOSE TEST TRACK 10 1KHz 0dB

Fig. 45. In/Out circuit diagram.

CIRCUIT DESCRIPTION 72

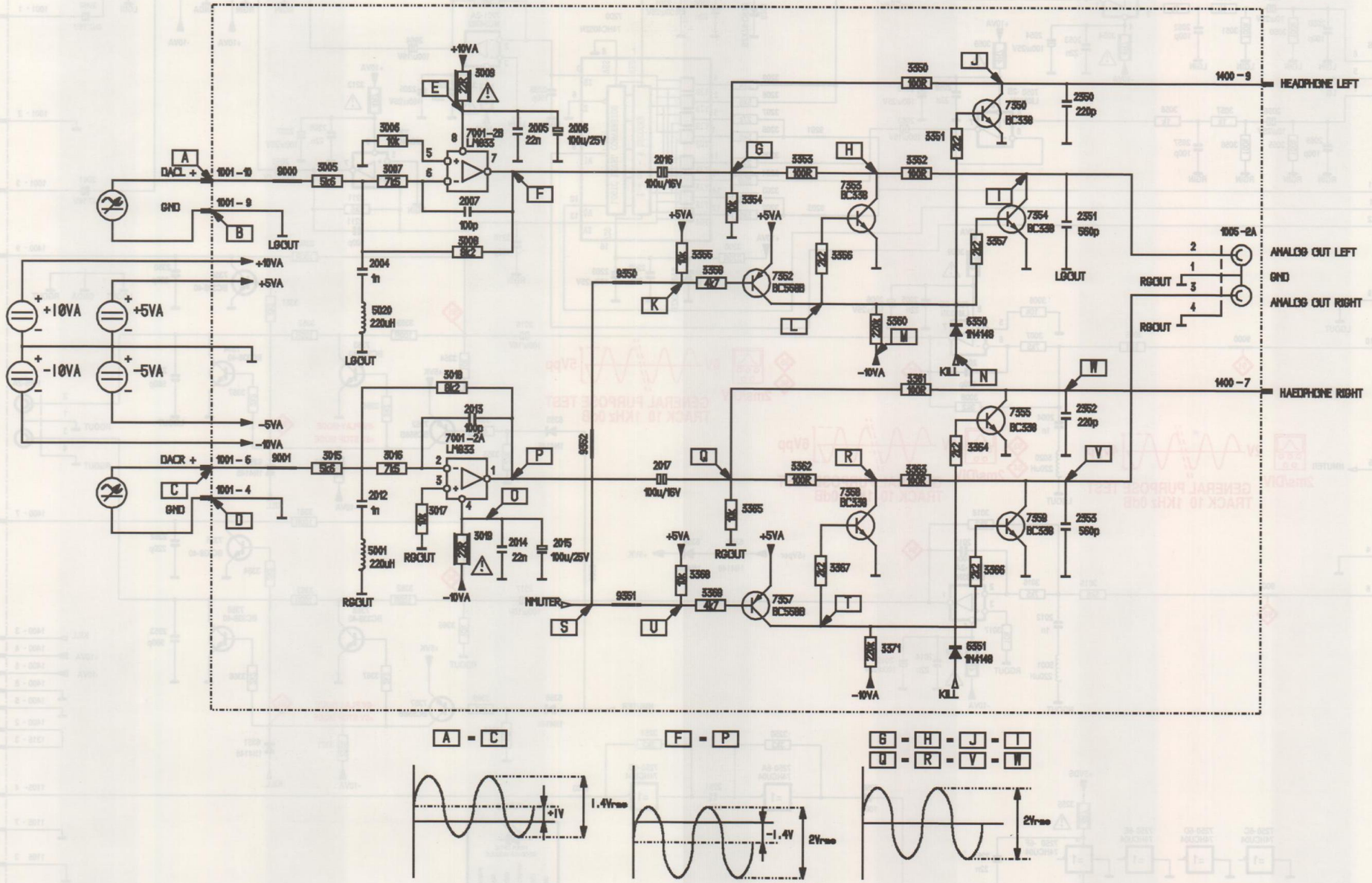

Fig. 46. Measuring lay-out analog output circuit.

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73 CIRCUIT DESCRIPTION

CONTROL & DISPLAY CIRCUIT DIAGRAM

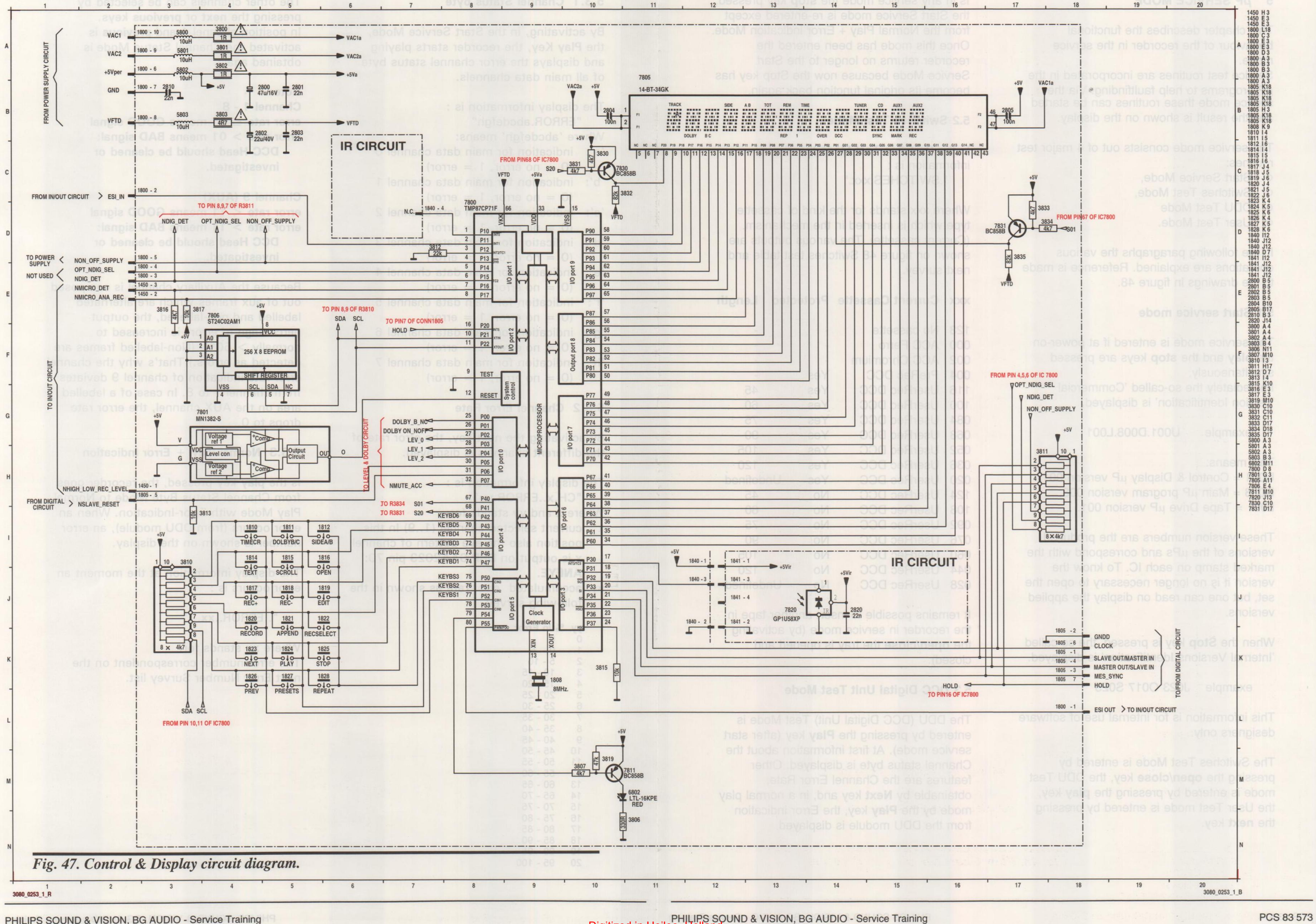


Fig. 47. Control & Display circuit diagram.

5 µP SERVICE MODE

This chapter describes the functional behaviour of the recorder in the service mode.
Service test routines are incorporated in the µP programs to help faultfinding. Via the service mode these routines can be started and the result is shown on the display.

The service mode consists out of 4 major test routines:
- Start Service Mode,
- Switches Test Mode,
- DDU Test Mode
- User Test Mode.

In the following paragraphs the various operations are explained. Reference is made to the drawings in figure 48.

5.1 Start service mode

The service mode is entered if at power-on the **play** and the **stop** keys are pressed simultaneously.
Immediately the so-called 'Commercial Version Identification' is displayed.

example U001.D008.L001

This means:
U001 = Control & Display µP version 001,
D008 = Main µP program version 008,
L001 = Tape Drive µP version 001.

These version numbers are the produced versions of the µPs and correspond with the marked stamp on each IC. To know the version it is no longer necessary to open the set, but one can read on display the applied versions.

When the **Stop** key is pressed, the so-called 'Internal Versions Identification' is displayed.

example J023 O017 S025

This information is for internal use of software designers only.

The Switches Test Mode is entered by pressing the **open/close** key, the DDU Test mode is entered by pressing the **play** key, the User Test mode is entered by pressing the **next** key.

Is in any service mode the **stop** key pressed, the Start Service mode is re-entered except from the Normal Play + Error indication Mode. Once this mode has been entered the recorder returns no longer to the Start Service Mode because now the Stop key has become its original function back again.

5.2 Switches Test Mode

In the Switches Test Mode the display information is :
".SWITCHES.xxx."

Where xxx stands for the kind of cassette type which is inserted in the mechanism. (Current cassette). The various outputs are shown on figure 48 Switches test table and next survey.

xxx	Current Cassette	Protected	Length
123	No cassette	-	-
000	ACC Ferro	-	-
002	ACC Chromium	-	-
004	PreRec DCC	Yes	-
116	UserRec DCC	Yes	45
100	UserRec DCC	Yes	60
084	UserRec DCC	Yes	75
068	UserRec DCC	Yes	90
052	UserRec DCC	Yes	105
036	UserRec DCC	Yes	120
020	UserRec DCC	Yes	Undefined
124	UserRec DCC	No	45
108	UserRec DCC	No	60
092	UserRec DCC	No	75
076	UserRec DCC	No	90
060	UserRec DCC	No	105
044	UserRec DCC	No	120
028	UserRec DCC	No	Undefined

It remains possible to insert another tape in the recorder in service mode (by activating the **open/close** the tray is opened and closed).

5.3 DCC Digital Unit Test Mode

The DDU (DCC Digital Unit) Test Mode is entered by pressing the **Play** key (after start service mode). At first information about the Channel status byte is displayed. Other features are the Channel Error Rate, obtainable by **Next** key and, in a normal play mode by the **Play** key, the Error indication from the DDU module is displayed.

CIRCUIT DESCRIPTION 74

5.3.1 Channel Status byte

By activating, in the Start Service Mode, the **Play** Key, the recorder starts playing and displays the error channel status byte of all main data channels.

The display information is :
"ERROR.abcdefgh"
Where 'abcdefgh' means:
'a': indication for main data channel 0 (0 = no error, 1 = error)
'b': indication for main data channel 1 (0 = no error, 1 = error)
'c': indication for main data channel 2 (0 = no error, 1 = error)
'd': indication for main data channel 3 (0 = no error, 1 = error)
'e': indication for main data channel 4 (0 = no error, 1 = error)
'f': indication for main data channel 5 (0 = no error, 1 = error)
'g': indication for main data channel 6 (0 = no error, 1 = error)
'h': indication for main data channel 7 (0 = no error, 1 = error)

5.3.2 Channel Error Rate

By activating the **next** key, the error rate of the different channels is displayed.

The display information is :
"CH.x..ERROR.yy"
Where x and yy stands for:
x : current selected channel (1..9) In this position also the eye pattern of channel x is output on DRP SAA2023 pin 70: **ANEYE**.
yy: accumulated error rate as shown in the following survey.

yy	% in Error
0	0
1	0 - 5
2	5 - 10
3	10 - 15
4	15 - 20
5	20 - 25
6	25 - 30
7	30 - 35
8	35 - 40
9	40 - 45
10	45 - 50
11	50 - 55
12	55 - 60
13	60 - 65
14	65 - 70
15	70 - 75
16	75 - 80
17	80 - 85
18	85 - 90
19	90 - 95
20	95 - 100

The other channels can be selected by pressing the **next** or **previous** keys.
In position channel 1 and **previous** is activated the Channel Status Mode is obtained again.

Note:
Channel 1 - 8
error rate ≤ 01 means GOOD signal
error rate > 01 means BAD signal:
DCC Head should be cleaned or investigated.

Channel 9 (AUX)
error rate < 11 means GOOD signal
error rate > 11 means BAD signal:
DCC Head should be cleaned or investigated.

Because the Auxiliary channel is composed out of aux frames which are alternated labelled and non-labelled, the output percentage of errors is increased to normally > 50%. (Non-labelled frames are detected as errors.) That's why the channel error rate indication of channel 9 deviates from channel 1 to 8. In case of a labelled area on the AUX channel, the error rate drops to 0.

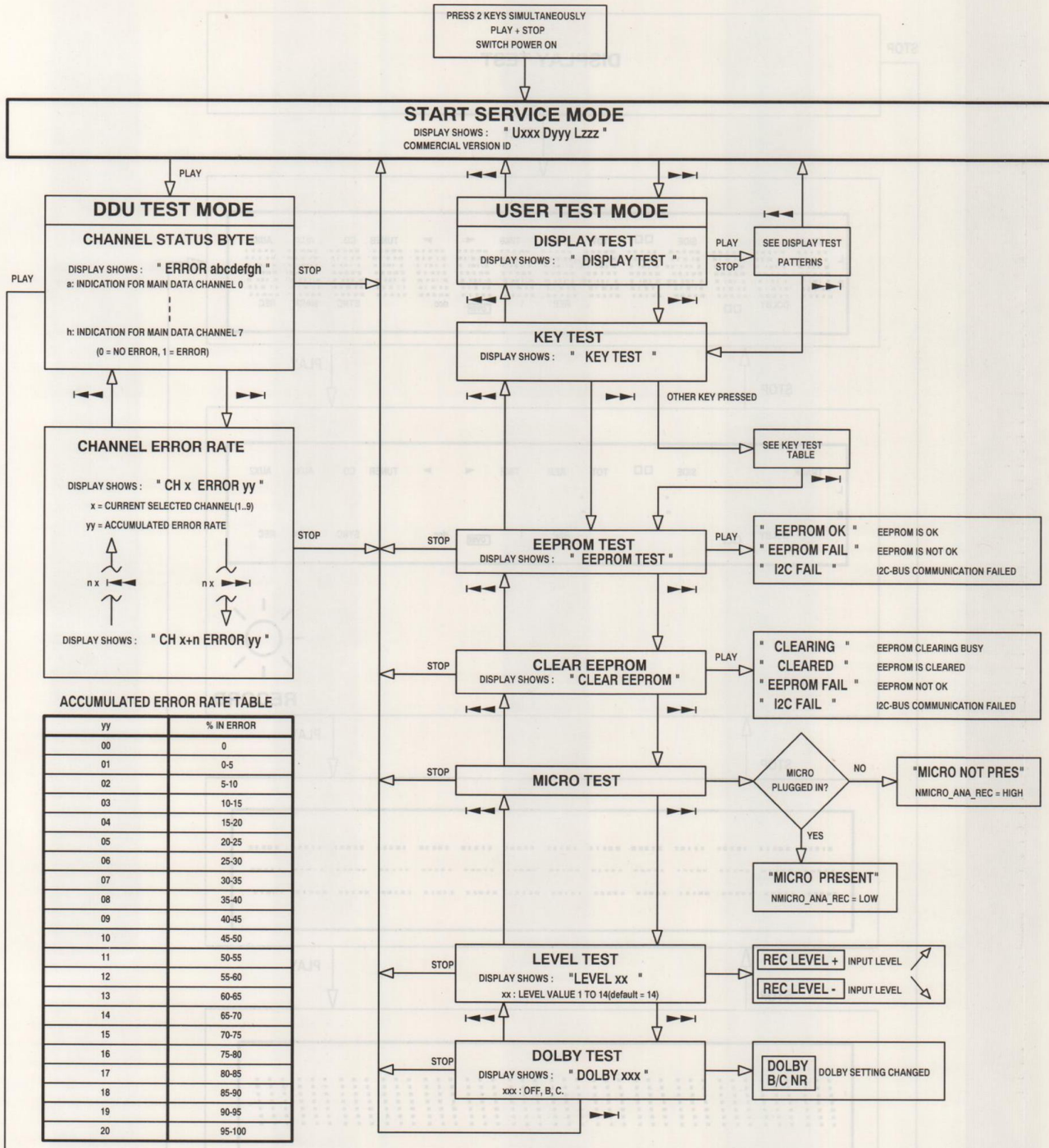
5.3.3 Normal Play + Error Indication

Is the **play** key pressed, the recorder goes from Channel Status Byte Mode to Normal Play Mode with Error-Indication. When an error occurs (from DDU module), an error number is shown on the display.

The display information at the moment an error occurs is :

"..ERROR..**xx**..."

Where **xx** stands for:
The error number correspondent on the next Error Number Survey list.



ACCUMULATED ERROR RATE TABLE

yy	% IN ERROR
00	0
01	0-5
02	5-10
03	10-15
04	15-20
05	20-25
06	25-30
07	30-35
08	35-40
09	40-45
10	45-50
11	50-55
12	55-60
13	60-65
14	65-70
15	70-75
16	75-80
17	80-85
18	85-90
19	90-95
20	95-100

SWITCHES TEST TABLE

xxx	CURRENT CASSETTE	PROTECTED	LENGTH
123	NO CASSETTE	-	-
000	ACC FERRO	-	-
002	ACC CHROMIUM	-	-
004	PRE RECORDED DCC	YES	-
116	USER RECORDED DCC	YES	45
100	USER RECORDED DCC	YES	60
084	USER RECORDED DCC	YES	75
068	USER RECORDED DCC	YES	90
052	USER RECORDED DCC	YES	105
036	USER RECORDED DCC	YES	120
020	USER RECORDED DCC	YES	UNDEFINED
124	USER RECORDED DCC	NOT	45
108	USER RECORDED DCC	NOT	60
092	USER RECORDED DCC	NOT	75
076	USER RECORDED DCC	NOT	90
060	USER RECORDED DCC	NOT	105
044	USER RECORDED DCC	NOT	120
028	USER RECORDED DCC	NOT	UNDEFINED

REMARK ERROR RATE

CHANNEL 1 - 8	ERROR RATE = < 01 : GOOD	
	ERROR RATE > 01 : BAD	PLEASE CLEAN OR INVESTIGATE HEAD
CHANNEL 9 (AUX)	ERROR RATE = < 11 : GOOD	
	ERROR RATE > 11 : BAD	PLEASE CLEAN OR INVESTIGATE HEAD

HAS1132
9424

Fig. 48. Flow Chart Service Test Program.

KEY TEST TABLE

KEY TEST

REMOTE KEY PRESSED

DISPLAY SHOWS : "REMOTE KEY xxx"

XXX	KEY ON REMOTE
011	TIME
047	SIDE A/B
028	REPEAT
054	STOP
053	PLAY
040	REC SELECT/PAUSE
117	APPEND
55	RECORD
121	EDIT
103	REC LEVEL -
102	REC LEVEL +
045	OPEN/CLOSE
015	SCROLL/DEMO
122	TEXT
001	1 (ABC)
002	2 (DEF)
003	3 (GHI)
004	4 (JKL)
005	5 (MNO)
006	6 (PQR)
007	7 (STU)
008	8 (VWX)
009	9 (YZ_)
000	0 (-+*)
063	DCC
012	STANDBY
052	FORWARD
050	BACKWARD

FRONT KEY PRESSED

DISPLAY SHOWS : "PRESSED KEY xx"

XX	KEY ON FRONT
13	TIME
07	DOLBY B/C NR
01	SIDE A/B
06	REPEAT
12	PRESETS
05	STOP
11	PLAY
04	REC SELECT/PAUSE
10	APPEND
16	RECORD
03	EDIT
09	REC LEVEL -
15	REC LEVEL +
02	OPEN/CLOSE
08	SCROLL
14	TEXT

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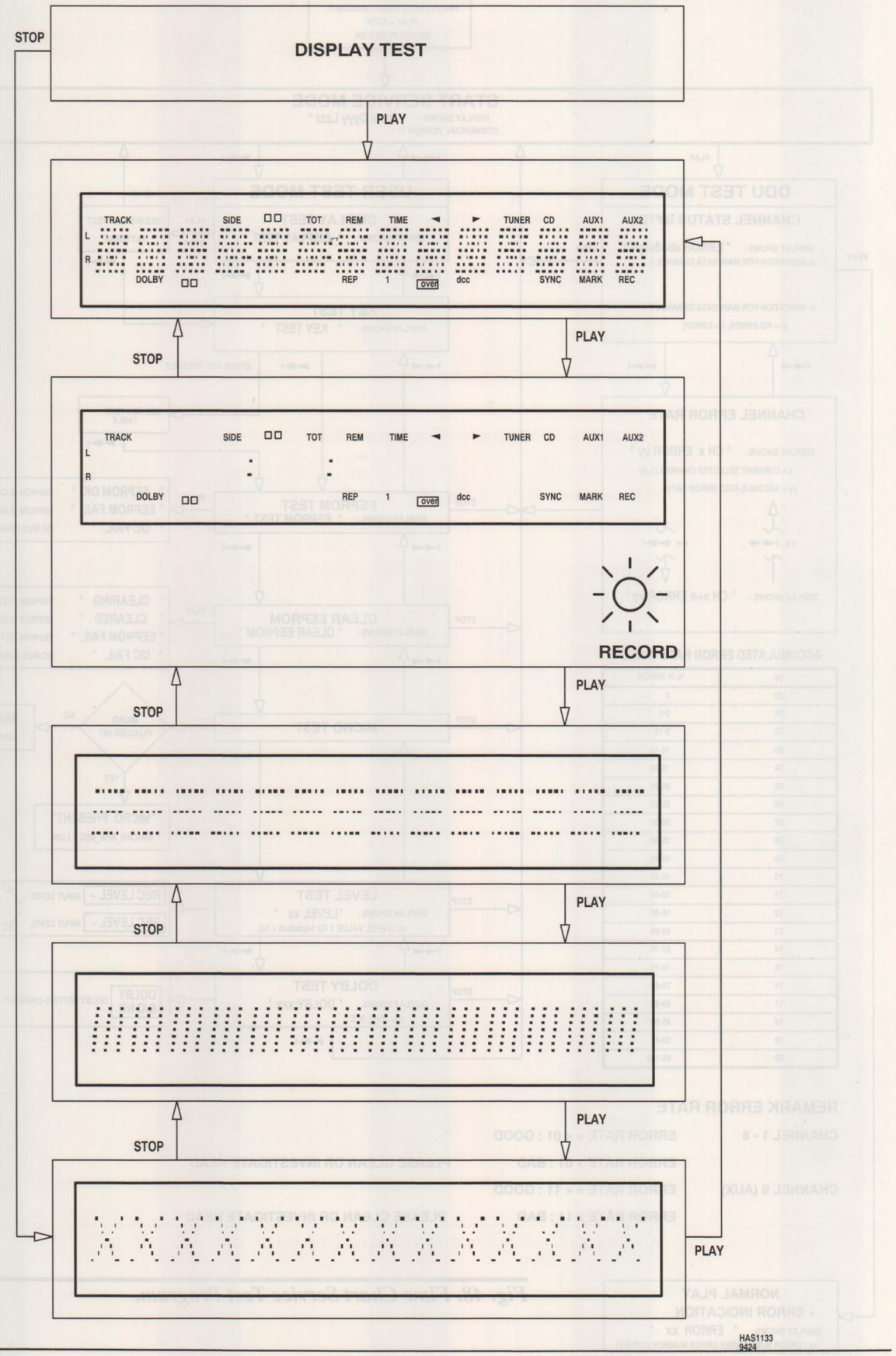
Fig. 49. Service Mode: Key Test Table and Display Test Patterns.

DISPLAY TEST PATTERNS



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ERROR NUMBER SURVEY LIST

00 = No error

01 = Deck failed
The requested command could not be executed because of a malfunctioning of the mechanics.

02 = Tray blocked
This error is issued when the tray has been blocked, although the tray might be moving out again due to this fact. The blocked indication will hence occur very short in the tray status message and could be missed.

03 = Tray pulled open
During normal operation the tape drive module has sensed that the tray loader is forced to the open state by the user.

04 = Invalid parameter
The parameter going with the last received command is unknown or out of range.

05 = No cassette
The command can not be executed since there is no cassette loaded.

06 = Digital Audio input out of lock or missing carrier frequency.
During recording from a digital input, no input signal is detected. When continuing the recording, undefined data will be recorded which may lead to unpredictable audio during playback. The DDU module will refuse to continue the recording.

07 = Digital Audio input has Professional class (unsupported)
During recording from a digital input, a professional source may be detected which is not supported by the DDU module, hence the module will refuse to record from this source.

08 = Digital Audio input has non-audio format
During recording from a digital input, the input data may contain computer data instead of audio. The DDU module will refuse to continue the recording.

09 = Copy right protection violation (SCMS)
During recording from a digital input, which contains user audio data but which is copyright protected, the DDU module will refuse to continue the recording.

11 = Record attempted on write protected tape
A record or auxiliary record or record-pause command is issued while the loaded cassette is write protected or is an ACC. The DDU module will refuse to record on such a tape.

13 = Invalid command received
The command which was received is not allowed in this context.

15 = Command overrun
The DDU module has received to many state changing commands in a row to handle. This error occurs whenever a command is received while another command is still waiting for execution. The DDU module will not store a queue of received commands.

16 = Signature not yet loaded
The record command will only be accepted by the DDU module after the setmakers signature has been loaded. This will make it possible to identify the recording set of each DCC cassette.

17 = Unreliable TOC
During the process of TOC search the DDU module finds that the contents of the TOC does not match the contents of the tape. The search command should be repeated using relative search.

18 = Search target could not be found
The requested search target was valid but could not be found,
e.g. a direct track search after track number 5 on a super-user tape while track number 5 was removed by after-recording,
or an append search on a full tape is desired.

19 = Marker writing not allowed
A request for a marker can be rejected because of the fact that the last recorded marker is not yet 8 tape frames past or a marker is currently being written or the tape is write protected. Also when the requested marker is out of context (lead_in A on side B or reverse maker on side B) this error occurs.

20 = Not Used.

22 = No proper super-user tape
The renumber function could not detect a marker on this super user tape or the renumber function was called on a user tape.

23 = No TOC available
A direct access search has been requested on a super-user tape which does not have a valid TOC. This search request can not be honoured.

24 = Sector not allowed
Not allowed to change sector in this mode or a sector is requested which is not on the tape,
e.g. sector D on a 2-sector tape.

25 = No user characters loaded
An attempt to record user characters while these are not yet loaded.

26 = Clean head
The reproduction of the audio is bad due to dirt on the head. The user should clean it.

27 = Marker may not be removed
Attempt to erase a temporary reverse marker or the first start marker on the tape.

30 = Tape fault on tape broken/blocked.

31 = Power down detected by tape drive board.

34 = Renumber time out
Marker with abnormal length found, or virgin

tape is used, or End of Tape is reached.

35 = Tape full
Indication in append mode when no more room on tape is left.

5.4 The User Test Mode

The User Test Mode consists out of some minor modes. They are walked through by pressing the **next** or **previous** keys, starting from the Start Service Mode.

The Display Test

The display information is :
".DISPLAY.TEST."

If now the **previous** key is pressed, the Start Service Mode is re-entered.
If now the **next** key is pressed, the Key Test Mode is entered.

Key Test Mode

There are 5 display patterns available, figures 50 to 54. The patterns can be scrolled forward respectively backward by pressing the **play** respectively **stop** key. In pattern 2 also the record led is switched on.

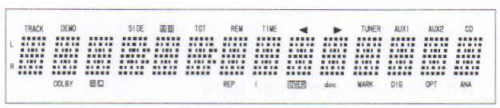

Fig. 50 Display pattern 1

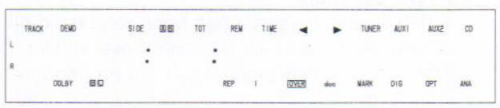

Fig. 51 Display pattern 2

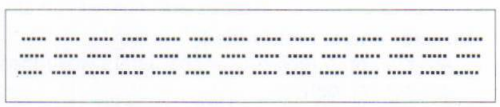

Fig. 52 Display pattern 3

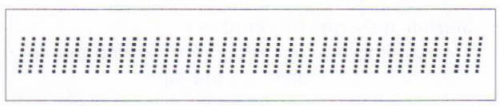

Fig. 53 Display pattern 4

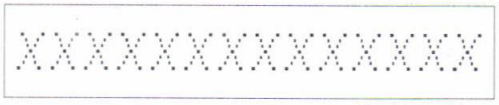

Fig. 54 Display pattern 5

The Key Test

The display information is :
"...KEY.TEST..."

If now the **previous** key is pressed, the Display Test Mode is entered.
If now the **next** key is pressed, the EEProm Test Mode is entered.

By activating all other keys on the front, the display information is :

"PRESSED.KEY.**xx**"
xx : depending pressed key as shown in the following survey:

xx	Key on front
13	time
07	dolby nr
01	side A/B
06	repeat
12	presets
05	stop
11	play
04	rec select/pause
10	append
16	record
03	edit
09	rec -
15	rec +
02	open/close
08	scroll/demo
14	text

By activating all other keys on the remote, the display information is :

"REMOTE..KEY.**xxx**"
xxx : depending pressed key as shown in the following survey:

xxx	Key on remote
011	time
047	side A/B
028	repeat
054	stop
053	play
040	rec select/pause
117	append
55	record
121	edit
103	rec -
102	rec +
045	open/close
015	scroll/demo
122	text
001	1 (ABC)
002	2 (DEF)
003	3 (GHI)
004	4 (JKL)
005	5 (MNO)
006	6 (PQR)
007	7 (STU)
008	8 (VWX)
009	9 (YZ_)
000	0 (-+*)
063	dcc
012	standby
052	forward
050	backward

The EEProm Test
The display information is :
"..EEPROM.TEST."

If now the **previous** key is pressed, the Key Test Mode is entered.
If now the **next** key is pressed, the Clear EEProm Mode is entered.
If now the **play** key is pressed, the EEProm test is executed which results in one of the following messages on the display:
"...EEPROM.OK.."
if the EEProm is ok.
".EEPROM.FAIL.."
if the EEProm is not ok.
"...I2C.FAIL..."
if the I²C-bus communication failed.

The Clear EEProm
The display information is :
".CLEAR.EEPROM."

If now the **previous** key is pressed, the EEProm Test Mode is re-entered.
If now the **next** key is pressed, the Micro Test Mode is entered.
If now the **play** key is pressed, the EEProm will be cleared and results in one of the following messages on the display:
"...CLEARING..."
if the EEProm clearing is busy.
"....CLEARED..."
if the EEProm is cleared.
"..EEPROM.FAIL.."
if the EEProm is not ok.
"...I2C.FAIL..."
if the I²C-bus communication failed.

The Micro(phone) Test
The display information is :
"MICRO.NOT.PRES"
if the microphone is not connected.
"MICRO..PRESENT"
if the microphone is connected.

Also the output line NMICRO_ANA_REC is switched to High if no microphone is connected in. If a microphone is connected, the NMICRO_ANA_REC output line is switched to Low.

If now the **previous** key is pressed, the EEProm test mode is entered.
If now the **next** key is pressed, the Level test mode is entered.

The Level Test
The display information is :
"...LEVEL.xx..."
xx: level value 1 to 14
(default value = 14)
The input level can be decreased respectively increased by pressing the **rec-** respectively **rec+** key.
The corresponding level lines will be switched to the correct value.

If now the **previous** key is pressed, the Micro test mode is entered.
If now the **next** key is pressed, the Dolby test mode is entered.

The Dolby Test
The display information is :
"..DOLBY.xxx..."
xxx: OFF, B.., C..
The dolby setting can be changed by pressing the **dolby b/c nr** key.
The corresponding dolby lines will be switched to the correct value.

If now the **previous** key is pressed, the Level test mode is entered.
If now the **next** key is pressed, the Start Service mode is entered.

6 ABBREVIATIONS

+10VD	10 volt digital supply output
+5VA	+5 Volt analog supply
+5VD	5 Volt digital supply
70/120µs circuit	Selection in ACC mode for Chrome/Ferro tape
A0	Address SRAM; Address DRAM
A1	Address SRAM; Address DRAM
A1 0/RAS	Address SRAM; RAS DRAM
A1 1	Address SRAM
A1 2/PinO5	Address SRAM; Address DRAM; Port expander output 5
A1 3/PinO2	Address SRAM; Address DRAM; Port expander output 2
A1 4/PinO1	Address SRAM; Address DRAM; Port expander output 1
A1 5/PinO4	Address SRAM; Address DRAM; Port expander output 4
A1 6/PinO3	Address SRAM; Address DRAM; Port expander output 3
A2	Address SRAM; Address DRAM
A3	Address SRAM; Address DRAM
A4	Address SRAM; Address DRAM
A5	Address SRAM; Address DRAM
A6	Address SRAM; Address DRAM
A7	Address SRAM; Address DRAM
A8	Address SRAM; Address DRAM
A9/CAS	Address SRAM; CAS for DRAM
A1+	Analog reader ACC Left channel
A2+	Analog reader ACC Right channel
ACC/NDCC	Analog or DCC playback
ACCL	ACC output Left
ACCR	ACC output Right
ADAS3	Adaptive Allocation and Scaling IC
ADC	Analog Digital Converter
ALP	Azimuth Locking Pins
AMS	Automatic Music selection on Analog Compact Cassette
ANAEYE	Analogue eye pattern output
ANAL	ACC output Left
ANAR	ACC output Right
ATSB	12 dB attenuation(active LOW)
ATTDAC	DAC attenuation control.
AUX channel	Auxiliary channel
AZCHK	channel 0 and channel 7 azimuth monitor.
BCK	bit clock input.
BIAS	Bias current for ADC
BIL	buffer op-amp inverting input for left channel.
BIR	buffer op-amp inverting input for right channel.
BOL	buffer op-amp inverting input for left channel.
BOR	buffer op-amp output for right channel.
CAP_A	Capstan motor control connection A
CAP_B	Capstan motor control connection B
CAPSTAN	Low output level switches the capstan motor on.
CAPSTAN+	Capstan motor + connection
CAPSTAN-	Capstan motor - connection
CEDC	system clock output.
CHMODE	use of channel status (0=professional use, 1=consumer use)
CHROME	Indication if a chrome analog cassette is inserted.
CHTST1	Channel test pin 1
CHTST2	Channel test pin 2
CKIN	system clock input.
CKSL1	clock selection 1
CKSL2	clock selection 2
CLAMP	Write current output
CLK22	22.5792 MHz buffered clock output of SFC3.
CLK24	24.576 MHz XTAL buffered clock output of SFC3.
CLKSEL	select system clock
CLOCK	Serial data clock from controller
CLOSE_TRAY	Tray motor connection (+10V = Open tray; 0V = Close tray)
CMRD	tape deck mechanism
COA	Common analog
COAXIAL IN	IEC958 high sensitive input
COD	Common digital
COPY	copyright status bit
CRO2/TRAY_OPEN	CRO2/FE cassette detection switch input if N_CASS_PRES = L L = FE; H = CRO2 if N_CASS_PRES = H L = tray fully opened, H = tray is not fully opened
CTRLMODE	select µP/stand-alone mode
D0	Data SRAM; Data DRAM
D1	Data SRAM; Data DRAM
D2	Data SRAM; Data DRAM
D3	Data SRAM; Data DRAM
D4	Data SRAM;
D5	Data SRAM;
D6	Data SRAM;
D7	Data SRAM;
DAC	Digital Analog Converter IC
DACL	Analog audio output left
DACR	Analog audio output right
DAIO	Digital Audio Input Output IC
DATA	data input
DCC_CASS_PRES	DCC cassette present switch input
DEEM	pre-emphasis output bit
DEEM1	de-emphasis on/off
DEEM2	de-emphasis on/off
DEEMDAC	DAC control output.
DIGITAL IN	IEC958 input signal

DIGITAL OUT	IEC958 output
DOLBY	Dolby noise reduction system
DRAM	Dynamic Random Access Memory IC
DRP	The DCC Drive Processor
DSMB	double speed mode (active LOW).
ERCOSTAT	ERCO status, for test only
FATG	Fixed Azimuth Tape Guides
FDAI	filtered serial data input (from ADAS)
FDAO	filtered serial data output (to ADAS)
FDCL	filtered data bit clock
FDIR	PASC mode encode/decode
FDWS	filtered data word select
FILTCL	capacitor for left channel 1st order filter function.
FILTCR	capacitor for right channel 1st order filter function.
FRESET	reset signal from codec.
FS256	master audio clock at 256 x sample frequency
FS32	indicates sample frequency = 32kHz
FS44	indicates sample frequency = 44kHz
FS48	indicates sample frequency = 48kHz
FSYNC	subband synchronisation on F-I^{2}S bus.
GNDA	Analog ground
GNDD	Digital ground
GNDS	Analog motors ground
HOLD	DDU is busy flag
HPEN	high pass filter enable input.
I^{2}S	I^{2}Sbus
I^{2}SOUTEN	serial audio output enable.
I^{2}SSEL	select auxiliary input or normal input in transmit mode.
IECIN0	TTL level IEC input.
IECIN1	high sensitivity IEC input.
IECO	digital audio output for optical and transformer link.
IECOEN	digital audio output enable
IECOP	IEC958 digital audio output.
IECSEL	select IEC input 0 or 1
IN 0-7	Head signals of main data channels
INAUX	Head signal of auxiliary data.
INL	Analog input signals from DCC head.
INMFL	Magnetic feedback amplifier input left.
INMFR	Magnetic feedback amplifier input right.
INR	Analog input signals from DCC head.
INVALID	validity of audio sample input/output
IREF	current reference node.
L3	L3-bus
L3CLK	L3 bus clock line
L3CLKC	codec interface clock
L3CLKM	microcontroller interface clock
L3DATA	L3 bus serial data line
L3DATAC	codec interface data
L3DATAM	microcontroller interface data
L3INT	L3 interrupt output
L3MODE	Mode line for L3 interface
L3MODEC	codec interface mode
L3MODEM	microcontroller interface mode
L3REF	L3 bus timing reference
LADDR	microprocessor interface address switch input
LCLK	microprocessor interface clock line input
LDATA	microprocessor interface data line input/output
LEFT INPUT	Analog audio input left
LMODE	microprocessor interface mode line input
LOWPOWER	Low power playback reset
LTCNT0	LT compatible interface mode control
LTCNT0C	SFC interface mode control
LTCNT1	LT compatible interface mode control
LTCNT1C	SFC interface mode control
LTL	Landscape Tray Loader
M0	(test mode input) connect to VDD
M1	(test mode input) connect to VDD
MAIN µP	Digital board microprocessor
MCLK	6.144 MHz clock output
MESSAGE_SYNC	Indication line of block transfers from digital board µP to front µP, see MESSYNC.
MESSYNC	Message synchronisation with front controller
MFL1	feedback amplifier output left 1
MFL2	feedback amplifier output left 2
MFR1	feedback amplifier output right 1
MFR2	feedback amplifier output right 2
MLE	Latch enable signal for digital filter
MRH	Magneto Resistive thin film Head
MSYNC	Message synchronisation from Tape drive board µP with Digital board µP
MUSB	muting(active LOW)
MUTE	audio mute input
MUTEDAC	DAC control or general purpose output
MUXAUX	Auxiliary multiplexer input
N_CASS_PRES	Cassette present switch input
N_DCC_REC_PROT	DCC record protect switch input
N_FAILP	Power fail(L = power failure)
N_FLAP_PRESENT	Flap loader present indication
N_HOLE3	DCC tape length indication switch input
N_HOLE4	DCC tape length indication switch input
N_HOLE5	DCC tape length indication switch input
N_PLAY_POS	Indication if head is in play position
N_QREV_PRES	Quick reverse sensor present
N_TRAY_IN	Tray switch input
NC	not connected
N_DDC_REC_PROT	DCC record protection switch input
N_MUTE	Mute for audio channels

	(active low)
NODONE	No done state selection
N_RESET	Master reset Digital Unit
OEN	Output Enable for RAM
OPEN_TRAY	Tray motor connection (+10V = Close tray; 0V = Open tray)
OPTICAL IN	IEC958 input from optical receiver
OUT0-7	Main data output 0 till 7 of read IC
OUTAUX	Auxiliary data output read IC
OUTL	Analog (CC) output left
OUTR	Analog (CC) output right
OVLD	overload indication output.
PASC	Precision Adaptive Sub-band Coding
PINO1	Port expander output 1
PinO2/SPEEDB	Port expander output 2 / PWM capstan control output for deck B
PLAY MAG	Connection to the solenoid on the DDU deck.
POR	Power On Reset
PRGSTAT	TFE3 program status, for test only (in DRP IC)
PWRDWN	enable power-down input in the standby mode Put DRP into power down mode
QA-QJ	Signal for write heads.
QUICK_REVERSE	Quick reverse input signal
R0+	Digital reader CH0(Hot)
R1+	Digital reader CH1(Hot)
R2+	Digital reader CH2(Hot)
R3+	Digital reader CH3(Hot)
R4+	Digital reader CH4(Hot)
R5+	Digital reader CH5(Hot)
R6+	Digital reader CH6(Hot)
R7+	Digital reader CH7(Hot)
RCfil	pin for PLL loop filter
RCint	pin for integrating capacitor
RDCLK	read clock input
RDMUX	Analogue multiplexed input from READ AMPLIFIER
RDSYNC	Synchronisation output for READ AMPLIFIER
RESET	Reset signal from Digital Unit controller
RESET_UP	Reset tape drive module µP
RESOL0	resolution selection 0
RESOL1	resolution selection 1
RIGHT INPUT	Analog audio input right
RSENSE	sense voltage positive input
RX+	Digital reader AUX channel(Hot)
RXD	Serial data input from tape drive unit
SB-I²S bus	DCC data forwarded via the SB-I²S bus
SBCL	Bit clock for sub-band I²S interface.
SBCL	sub-band bit clock
SBDA	Data line for sub-band I²S interface DRP
SBDIR	Direction line for sub-band I²S interface DRP
SBEF	Sub-band I²S error flag line
SBMCLK	Master clock for sub-band I²S interface DRP
SBWS	Word selector for sub-band I²S interface DRP.
SCK	I²S bus clock line
SCL	baseband bit clock
SCMS	Serial Copy Management System
SD	serial audio data input/output; I²S-bus
SDA1	baseband serial data to/from DAIO and ADC
SDA2	baseband serial data output to DAC
SDAD	Serial data from AD-converter
SDAUX	auxiliary serial data input; I²S-bus
SDDAC	I²S bus data line for DAC
SDO	serial interface data output.
SFC3	Stereo Filter and Codec IC
SFC3COMP	SFC3 compatibility mode
SFOR	input for selecting serial interface output format.
SHIELD	Shield connection
SLAVE	input for selecting serial interface operating mode MASTER/SLAVE.
SLAVE_IN	Serial data from controller
SLAVE_OUT	Serial data to controller
SPEED	PWM capstan control output for deck
SREEL	Tacho Supply reel
STANDBY	device inactive
STD	input for selecting STANDBY mode.
STROBE	strobe for control register (active high)
SUBSTR	Substrate connection
SWS	serial interface word select signal.
SYNCDAI	settings synchronisation for DAIO
SYSCLKI	system clock input
SYSCLKO	system clock output
TA1	Feedback conductor ACC Left channel
TA2	Feedback conductor ACC Left channel
TA8	Feedback conductor ACC Right channel
TA9	Feedback conductor ACC Right channel
TCLOCK	3.072 MHz clock output for tape I/O
TD1	Test conductor digital
TD2	Test conductor digital
TDAPLB	Control bits
TERAUX	Control bits
TEST0	test mode select
TEST1	test mode select
TEST2	Test mode select
TOC	Table of Contents of Sub-code information
TREEL	Tacho Take-up reel
TXD	Serial data output to tape drive unit
UDAVAIL	synchronisation for output user data (0 = data available, 1 = no data)
UNLOCK	PLL out-of-lock (0 = not locked, 1 = locked)
URDA	unreliable data from drive pro-

	cessing
VCCA	POSITIVE SUPPLY VOLTAGE CC-PART (+5V)
VCCM	POSITIVE SUPPLY VOLTAGE FEEDBACK AMPLIFIER (+5V)
VDACN	negative 1 bit DAC reference voltage input. (connected 0V)
VDACP	positive 1 bit DAC reference voltage input. (connected 5V)
VDD	POSITIVE SUPPLY VOLTAGE DCC-PART (+5V)
VddO	supply voltage (write outputs)
VEEA	ANALOG GROUND
VEED	DIGITAL GROUND
VEEM	GROUND FOR FEEDBACK AMPLIFIER
VOL	left channel output.
VOR	right channel output.
VREFD	VOLTAGE REFERENCE (DIGITAL)
VSS	SUPPLY GROUND (0V)
VssE	erase current source ground
VssS	sense voltage ground
W01	Digital writer(CH0/CH1)
W12	Digital writer(CH1/CH2)
W23	Digital writer(CH2/CH3)
W34	Digital writer(CH3/CH4)
W45	Digital writer(CH4/CH5)
W56	Digital writer(CH5/CH6)
W67	Digital writer(CH6/CH7)
W7-	Digital writer(CH7)
WCLK	write clock input
WDATA	Serial output to WRITE AMPLIFIER
WEN	Write enable for RAM
WIND+	Reel motor + connection
WIND-	Reel motor - connection
WRITE-STDBY	Write amplifier stand-by
WS	word select input/output, I^2S-bus
WX-	Digital writer(AUX channel)
WX0	Digital writer(AUX channel/CH0)
X22IN	22.5792 MHz XTAL oscillator input
X22OUT	22.5792 MHz XTAL oscillator output
X24IN	24.576 MHz XTAL oscillator input
X24OUT	24.576 MHz XTAL oscillator output
X256	master audio clock input from external source
Xin	system clock input